FAIRCHILD SEMICONDUCTOR®

September 2007

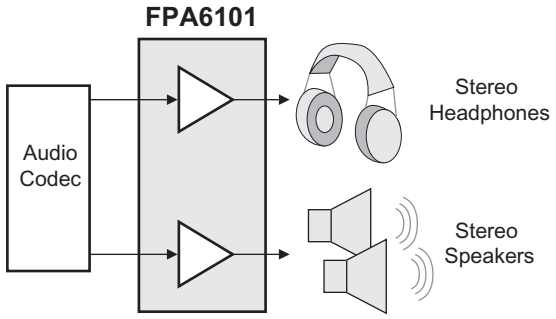
FPA6101
2.4W Stereo Audio Power Amplifier and Headphone Driver

Features

- Operating Voltage: V_{DD}, PV_{DD}, CV_{DD} = 4.5V to 5.5V
  HV_{DD} = 3.0V to 3.6V
- No Output Capacitors Required for Headphones
- Supply Current
  - I_{DD} = 12mA at V_{DD} = 5V (Amplifier Mode)
  - I_{DD} = 10mA at V_{DD} = 5V (Headphone Mode)
- Low Shutdown Current
- Meets VISTA Requirements
- Low Distortion

  AMP mode
  - THD+N = 56dB, R_L = 4Ω, P_O = 1.5W
  - THD+N = 64dB, R_L = 8Ω, P_O = 0.9W

  HP mode
  - THD+N = 73dB, R_L = 16Ω, P_O = 125mW
  - THD+N = 77dB, R_L = 32Ω, P_O = 88mW
  - THD+N= 85dB, R_L = 10kΩ, P_O = 1.7Vrms
- Integrated De-Pop Circuitry
- Thermal and Over Current Protection
- Internal Gain Setting
- High Supply Voltage Ripple Rejection
- Surface-Mount Packaging
  - TSSOP-28P (with enhanced thermal pad)
  - MLP-28P (with enhanced thermal pad) – Not yet released
- Lead Free Available (RoHS Compliant)



General Description

The FPA6101 is a monolithic integrated circuit combining a stereo power amplifier with a stereo capacitor-less headphone amplifier in a space and cost efficient package. The headphone amplifier is ground-referenced to eliminate the output capacitors saving money and PCB space.

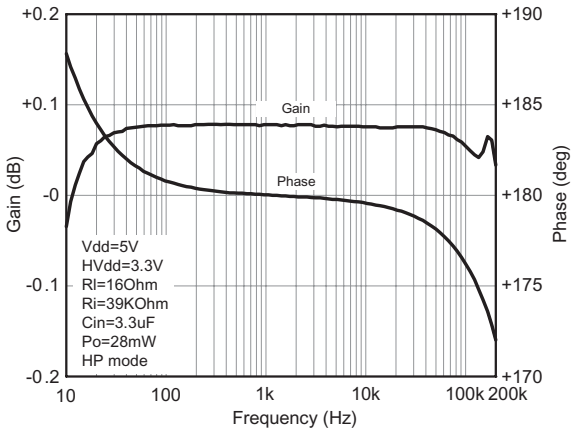
The amplifier features over-current, de-pop and thermal-shutdown protection. De-Pop reduces pops and clicks during power up and when using the shutdown modes. Thermal shut-down protects the amplifier from being destroyed by over-temperature or short-circuit failure.

Internal gain setting is provided to simplify the audio system design in notebook computer applications and can result in fewer support components and a reduction in PCB area. The FPA6101 is available in a TSSOP-28P or MLP-28P package. Both packages provide space saving and thermal efficiency.

Applications

- Note Book PCs
- LCD TVs and Monitors
- Portable DVD, CD, or HDTV players
- Portable Radios
- Portable Games

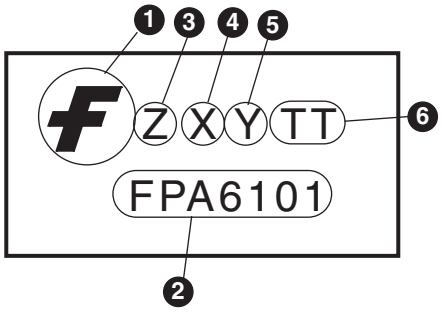
Frequency Response



Ordering and Marking Information

TSSOP-28 and MLP-28 Marking Information

Order Number	Package Number
FPA6101MTCX	TSSOP-28P
FPA6101MXL	MLP-28P



Definitions	
1	Fairchild logo
2	Device number
3	Assembly plant code
4	Year code

X	Alphabet
2000	A
2001	B
2002	C
2003	D
2004	E
2005	F
2006	G
2007	H
2008	J
2009	K
2010	A

5 — Six weeks numeric date code scheme

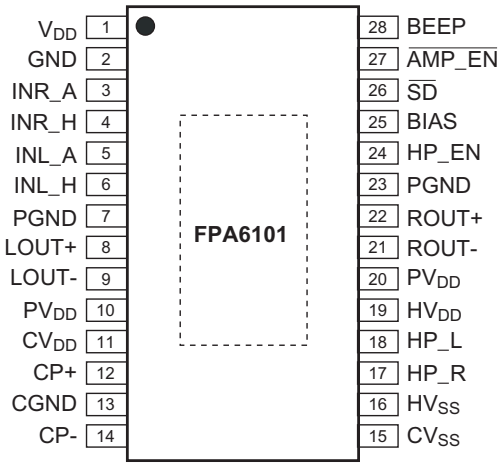
Work week No.	Y =
Work weeks 06–11	1
Work weeks 12–17	2
Work weeks 18–23	3
Work weeks 24–29	4
Work weeks 30–35	5
Work weeks 36–41	6
Work weeks 42–47	7
Work weeks 48–51	8
Work weeks 52–05	9

6	Die run code

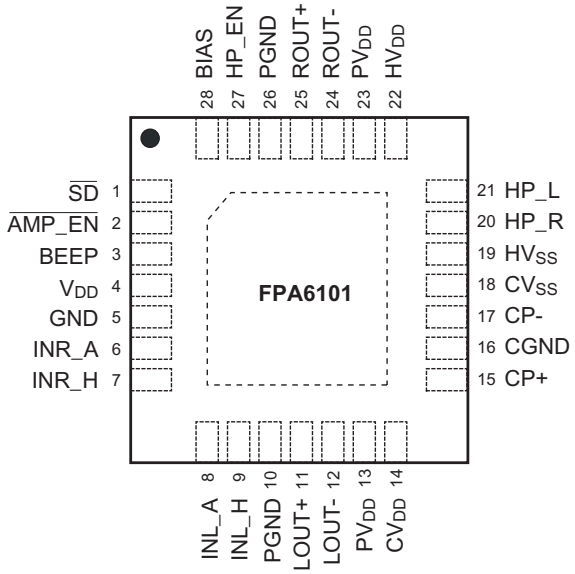
Note:

FAIRCHILD lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. FAIRCHILD lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configurations



TSSOP-28-P
(Top View)



MLP-28-P
(Top View)

⬚ = ThermaPad (connect the ThermalPad to GND plane for better heat dissipation)

Pin Description

TSSOP-28	MLP-28	Name	Function Description
1	4	V_{DD}	Power supply for control section
2	5	GND	Ground
3	6	INR_A	Right channel input terminal for speaker amplifier
4	7	INR_H	Right channel input terminal for headphone driver
5	8	INL_A	Left channel input terminal for speaker amplifier
6	9	INL_H	Left channel input terminal for headphone driver
7, 23	10, 26	PGND	Power ground
8	11	LOUT+	Left channel positive output for speaker
9	12	LOUT-	Left channel negative output for speaker
10, 20	13, 23	PV_{DD}	Power amplifier power supply
11	14	CV_{DD}	charge pump power supply
12	15	CP+	Charge pump flying capacitor positive connection
13	16	CGND	Charge pump ground
14	17	CP-	Charge pump flying capacitor negative connection
15	18	CV_{SS}	Charge pump output, connect to the “HVSS”
16	19	HV_{SS}	Headphone amplifier negative power supply
17	20	HP_R	Right channel output for headphone
18	21	HP_L	Left channel output for headphone
19	22	HV_{DD}	Headphone amplifier positive power supply
21	24	ROUT-	Right channel negative output for speaker
21	25	ROUT+	Right channel positive output for speaker
24	27	HP_EN	Headphone driver enable pin, pull HIGH to enable headphone mode
25	28	BIAS	Bias voltage generator
26	1	$\overline{SD}$	It will be into shutdown mode when pulled LOW, I_{SD} = 80μA
27	2	$\overline{AMP\_EN}$	Speaker driver enable pin, pull LOW to enable speaker mode
28	3	BEEP	PC BEEP trigger signal input

Block Diagram

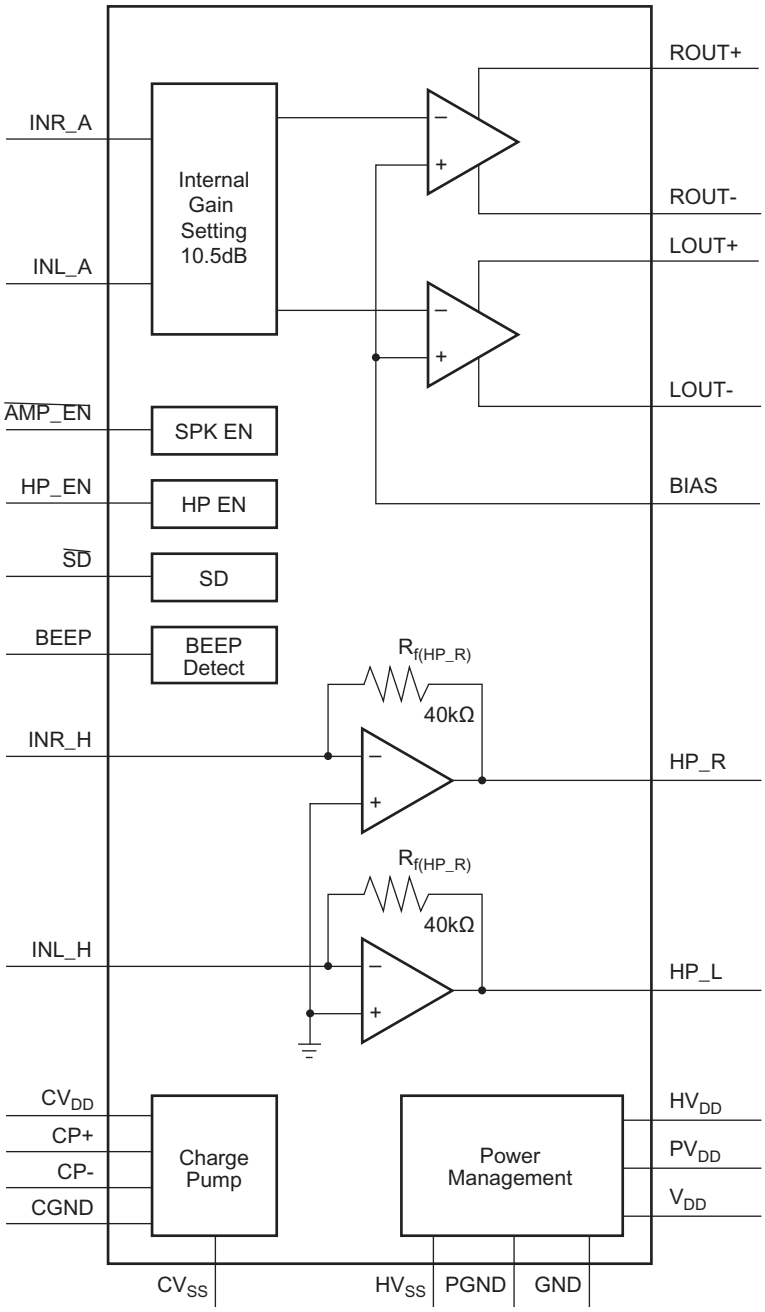


Figure 1.

Absolute Maximum Ratings(2)(3)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

(Over operating free-air temperature range unless otherwise noted)

Symbol	Parameter	Rating
PV_{DD}, V_{DD}, CV_{DD}	Supply Voltage	-0.3V to 6V
HV_{DD}	Supply Voltage	-0.3V to 4.6V
CV_{SS}, V_{SS}	Supply Voltage	+0.3V to -6V
$\overline{SD}$, $\overline{AMP\_EN}$, HP_EN	Input Voltage	0 to V_{DD} + 0.3V
T_A	Operating Temperature Range	-40°C to 85°C
$T_{J\ max}$	Maximum Junction Temperature	Internally Limited (°C)
T_{STG}	Storage Temperature Range	–65°C to +150°C
T_S	Soldering Temperature Range	260°C
V_{ESD}	Electrostatic Discharge	-2,000V to 2,000V(1) -200V to 200V(2)
P_D	Power Dissipation	Internally Limited (W)

Notes:

2. Human body model: C = 100pF, R = 1500Ω, 3 positives pulses plus 3 negative pulses.
3. Machine model: C = 200pF, L = 0.5F, 3 positive pulses plus 3 negative pulses.

Thermal Characteristics(4)

Symbol	Parameter	Rating
θ_{JA}	Thermal Resistance – Junction to Ambient	
	TSSOP-28P(4)	45°C/W
	MLP-28P(4)	45°C/W

Note:

4. 3.42 in^2 printed circuit board with 2oz. trace and copper through 10 vias of 15mil diameter vias. The thermal pad on the TSSOP-28P and MLP-28P packages with solder on the printed circuit board.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}, PV_{DD}, CV_{DD}	Supply Voltage		4.5	5.5	V
HV_{DD}			3.0	3.6	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$, $\overline{AMP\_EN}$, HP_EN	2		V
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$, $\overline{AMP\_EN}$, HP_EN		0.8	V
Vicm	Common Mode Input Voltage	for Amplifier	V_{DD} – 1		V
		for Headphone Amplifier	-0.7		

Electrical Characteristics

V_{DD} = PV_{DD} = CV_{DD} = 5V, HV_{DD} = 3.3V, GND = PGND = CPGND = 0V, T_A = 25°C (unless otherwise noted).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}, PV_{DD}	Supply Voltage		4.5		5.5	V
HV_{DD}	Headphone Amplifier Supply Voltage		3		3.6	V
CV_{DD}	Charge Pump Supply Voltage		4.5		5.5	V
I_{DD}	Supply Current	Only Speaker mode, $\overline{AMP\_EN}$ = HP_EN = 0V		18	30	mA
		Only Headphone mode, HP_EN = $\overline{AMP\_EN}$ = 5V		16	25	
		All Enable, HP_EN = 5V and $\overline{AMP\_EN}$ = 0V		23	40	
I_{SD}	Shutdown Current	$\overline{SD}$ = 0V		80	100	µA
I_I	Input Current	$\overline{SD}$, $\overline{AMP\_EN}$		1		µA
		HP_EN		10	15	
SPEAKER MODE, T_A = 25°C						
P_O	Output Power	THD = 1%, f = 1kHz:				W
		R_L = 4Ω		1.9		
		R_L = 8Ω	1.0	1.2		
		THD = 10%, f = 1kHz:				
		R_L = 4Ω		2.4		
		R_L = 8Ω	1.3	1.5		
V_{OS}	Output Offset Voltage	R_L = 8Ω, Gain = 10.5dB			10	mV
THD+n	Total Harmonic Distortion Plus Noise	f: 1kHz:				%
		P_O = 1.5W, R_L = 4Ω		0.15		
		P_O = 0.9W, R_L = 8Ω		0.06		
X'talk	Channel Separation	f = 1kHz, Cb = 2.2mF, R_l = 8Ω, P_O = 0.92W		80		dB
		f = 1kHz, Cb = 2.2mF, R_l = 4Ω, P_O = 1.5W		83		
PSRR	Power Supply Rejection Ratio	Cb = 2.2µF, R_L = 8Ω, f = 120Hz		70		dB
S/N		P_O = 0.8W, R_L = 8Ω, A-weighted Filter		90		dB
V_n	Noise Output Voltage	Gain = 10.5dB, R_L = 8Ω, Cb = 2.2µF		80		µV (rms)
A_V	Internal Voltage Gain	Amplifier mode, No load	10	10.5	11	dB
Ri	Input Resistance		16	18	20	kΩ

Electrical Characteristics (Continued)

V_{DD} = PV_{DD} = CV_{DD} = 5V, HV_{DD} = 3.3V, GND = PGND = CPGND = 0V, T_A = 25°C (unless otherwise noted).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
HEADPHONE MODE, T_A = 25°C						
Po	Output Power	THD = 1%, f = 1kHz:				mW
		R_L = 16Ω			160	
		R_L = 32Ω		100	120	
		THD = 10%, f = 1kHz:				
		R_L = 16Ω			200	
		R_L = 32Ω		150	165	
V_O	Output Voltage Swing	R_l = 10kΩ:				Vrms
		THD = 10%			2.9	
		THD = 1%			2.4	
V_{OS}	Output Offset Voltage	RL = 32Ω	-10		+10	mV
THD+n	Total Harmonic Distortion plus Noise	f = 1kHz:				%
		P_O = 125mW, RL = 16Ω		0.02		
		P_O = 88mW, RL = 32Ω		0.02		
		V_O = 1.7Vrms, RL = 10kΩ		0.005		
X'talk	Channel Separation	f = 1kHz, R_l = 16Ω, P_O = 125mW		85		dB
		f = 1kHz, R_l = 32Ω, P_O = 88mW		95		
		f = 1kkHz, R_l = 10kΩ, V_O = 1.7Vrms		100		
PSRR	Power Supply Rejection Ratio	C_B = 2.2µF, R_L = 32Ω, f = 120Hz		80		dB
S/N		With A-weighted Filter				dB
		P_O = 70mW, R_L = 32Ω		95		
		VO = 1.2Vrms, R_L = 10kΩ		92		
Vn	Noise Output Voltage	C_B = 2.2µF		30		µV (rms)
Rf	Input Feedback Resistance		38	40	42	kΩ
CHARGE PUMP						
Fosc	Switching Frequency		460	540	620	kHz
CVss		No load		-0.98 CV_{DD}		V
Req	Charge Pump Requirement Resistance			9	10	Ω
BEEP						
Vbeep	Beep Trigger Level			3		V_{PP}
T_{RES}	Beep Response Time			4		mS

Electrical Characteristics (Continued)

V_{DD} = PV_{DD} = CV_{DD} = 5V, HV_{DD} = 3.3V, GND = PGND = CPGND = 0V, T_A = 25°C (unless otherwise noted).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ATTENUATION						
HP_EN	HP Disable Attenuation	R_L = 32Ω, V_O = 1.1Vrms, fin = 1kHz		110		dB
		R_L = 10kΩ, V_O = 1.1Vrms, fin = 1kHz		85		
$\overline{AMP\_EN}$	AMP Disable Attenuation	R_L = 8Ω, V_O = 2Vrms, fin = 1kHz		112		dB
		R_L = 4Ω, V_O = 2Vrms, fin = 1kHz		112		
$\overline{SD}$	Shutdown Active	R_L = 10kΩ, V_O = 1.1Vrms, fin = 1kHz		90		dB
		R_L = 8Ω, V_O = 1Vrms, fin = 1kHz		100		
HEADPHONE TO SPEAKER CROSSTALK						
X'talk	Channel Separation	$\overline{AMP\_EN}$ = 0, R_L = 8Ω		85		dB
		HP_EN = 1, R_L = 16Ω, fin = 1kHz, P_O = 125mW		85		
SPEAKER TO HEADPHONE CROSSTALK						
X'talk	Channel Separation	$\overline{HP\_EN}$ = 1, R_L = 10kΩ		80		dB
		$\overline{AMP\_EN}$ = 0, R_L = 4Ω, fin = 1kHz, P_O = 1.5W		80		

Typical Operating Characteristics

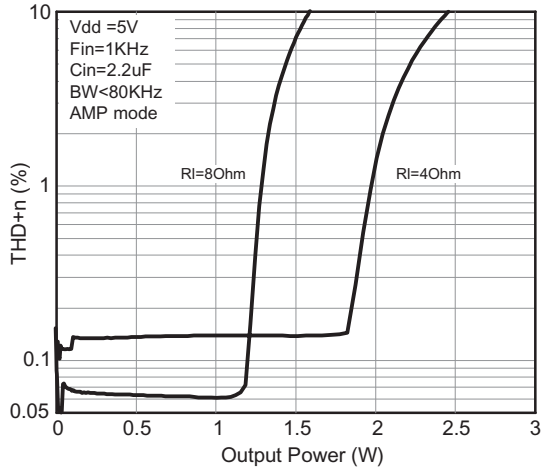


Figure 2. THD+n vs. Output Power

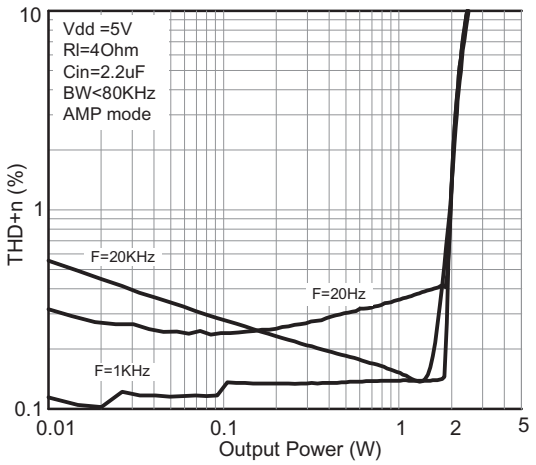


Figure 3. THD+n vs. Output Power

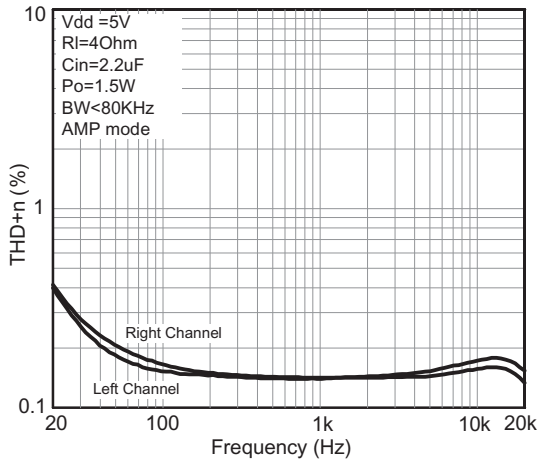


Figure 4. THD+n vs. Frequency

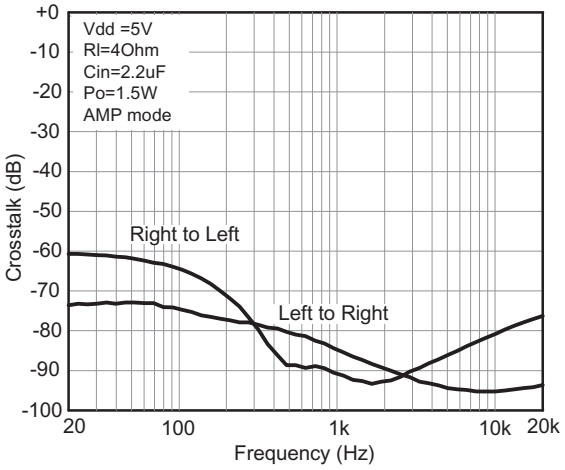


Figure 5. Crosstalk vs. Frequency

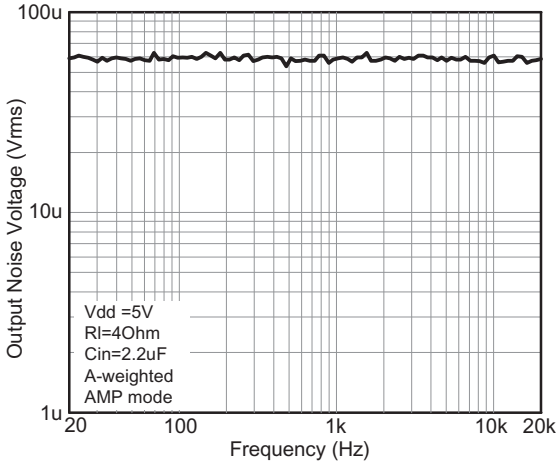


Figure 6. Output Noise Voltage vs. Frequency

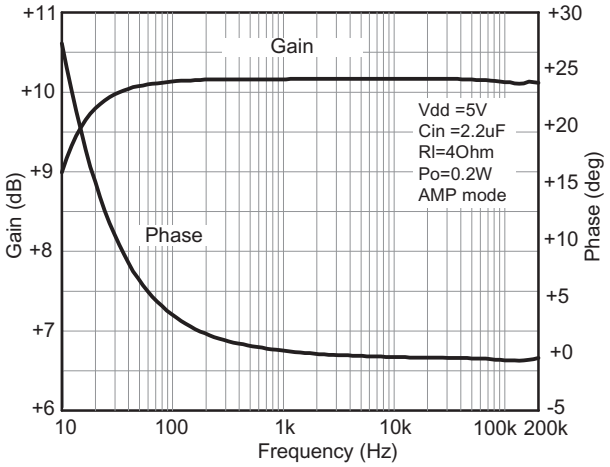


Figure 7. Frequency Response

Typical Operating Characteristics (Continued)

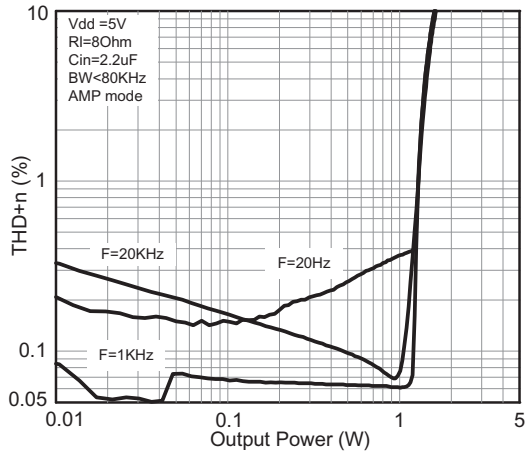


Figure 8. THD+n vs. Output Power

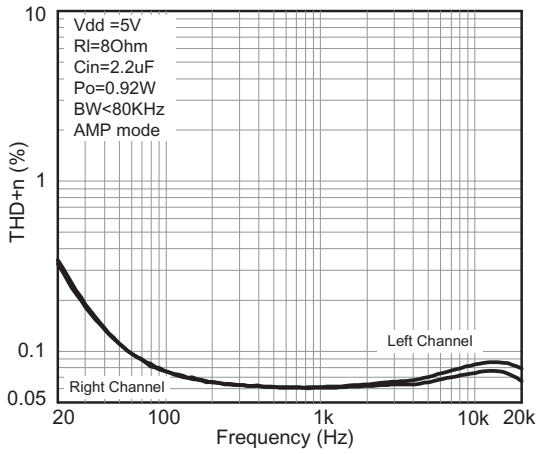


Figure 9. THD+n vs. Frequency

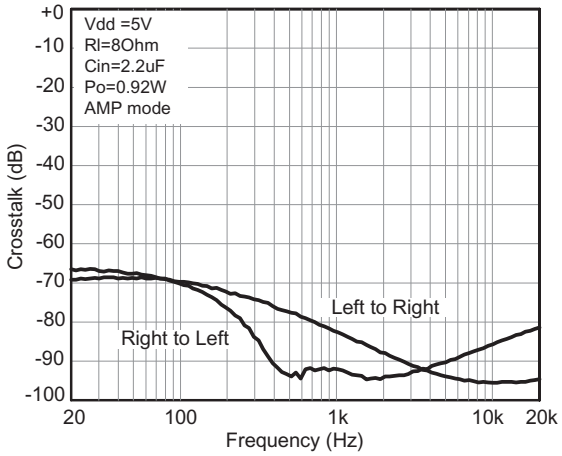


Figure 10. Crosstalk vs. Frequency

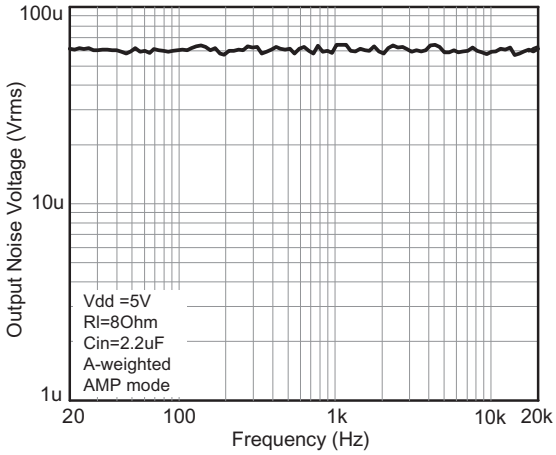


Figure 11. Output Noise Voltage vs. Frequency

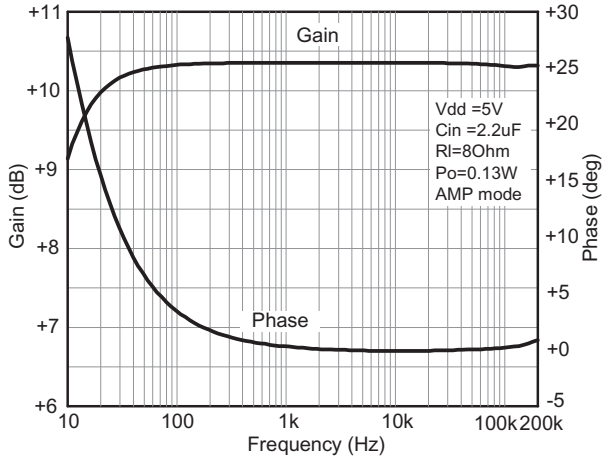


Figure 12. Frequency Response

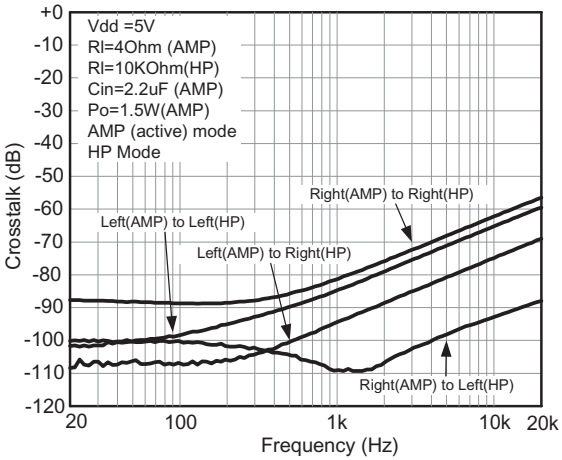


Figure 13. Crosstalk vs. Frequency

Typical Operating Characteristics (Continued)

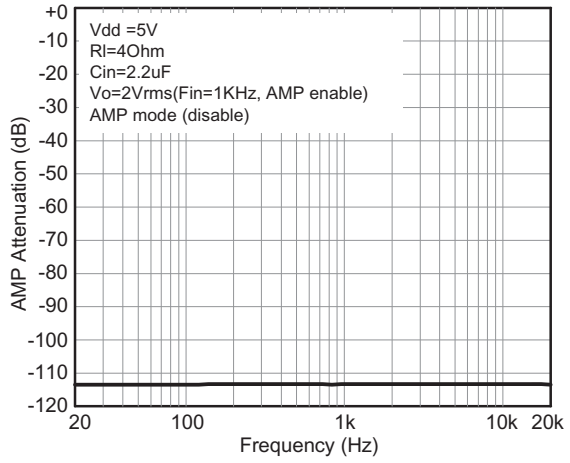


Figure 14. AMP Attenuation vs. Frequency

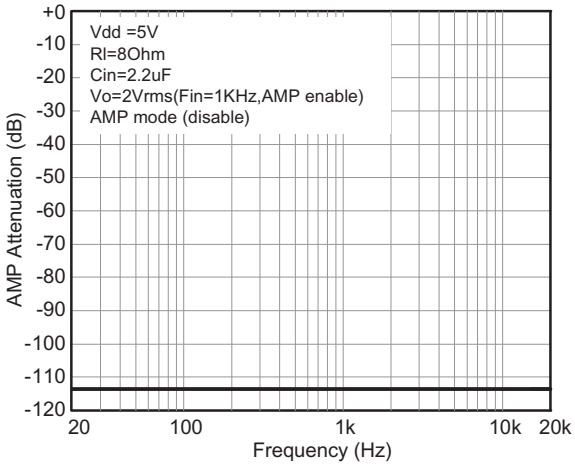


Figure 15. AMP Attenuation vs. Frequency

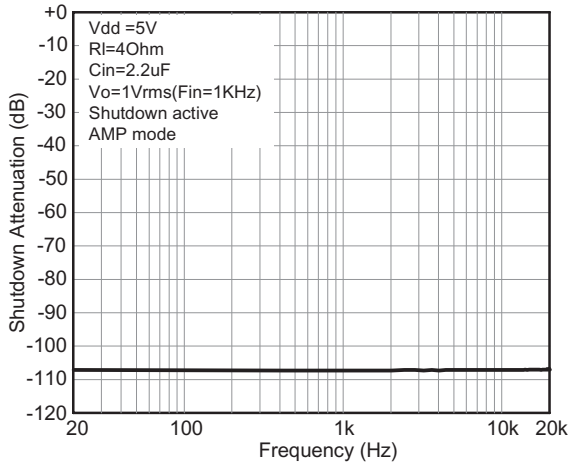


Figure 16. Shutdown Attenuation vs. Frequency

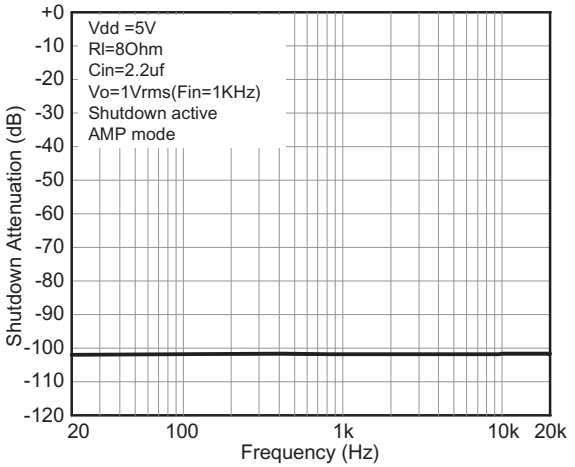


Figure 17. Shutdown Attenuation vs. Frequency

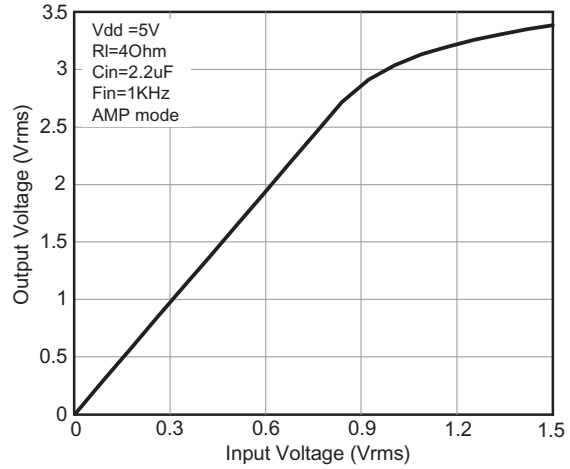


Figure 18. Input Voltage vs. Output Voltage

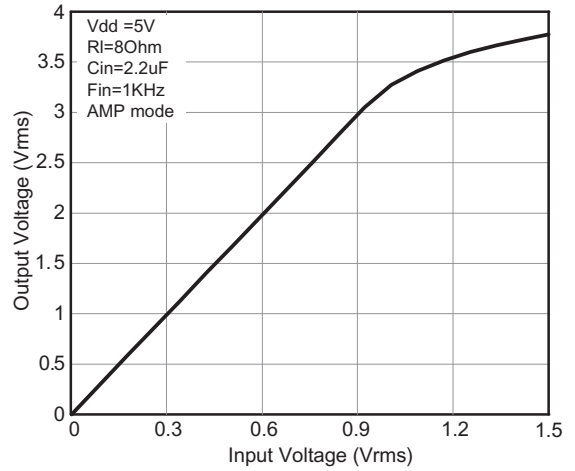


Figure 19. Input Voltage vs. Output Voltage

Typical Operating Characteristics (Continued)

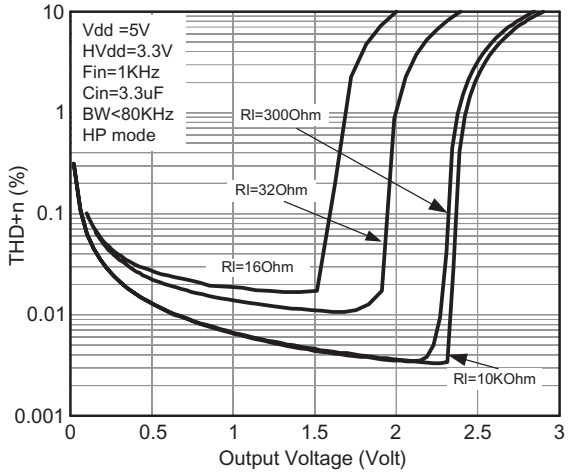


Figure 20. THD+n vs. Output Voltage

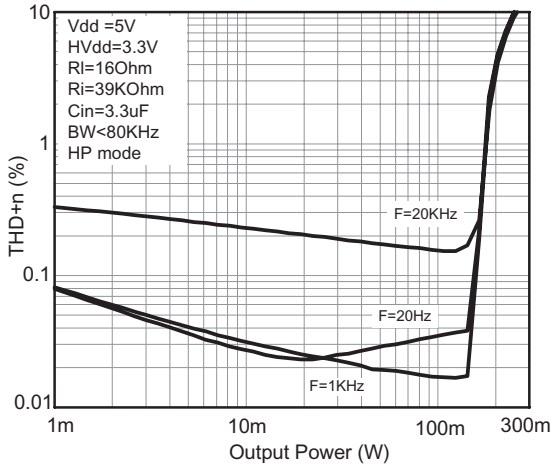


Figure 21. THD+n vs. Output Power

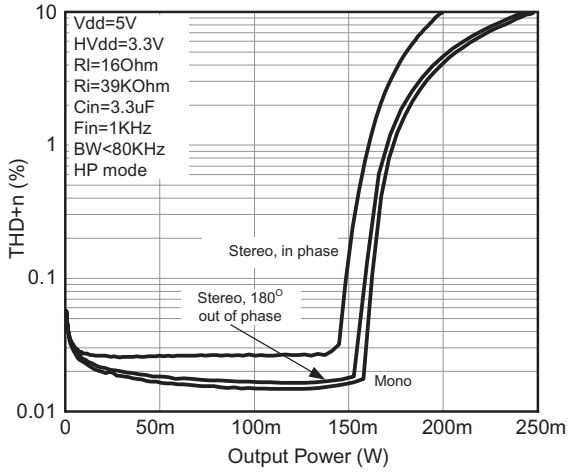


Figure 22. THD+n vs. Output Power

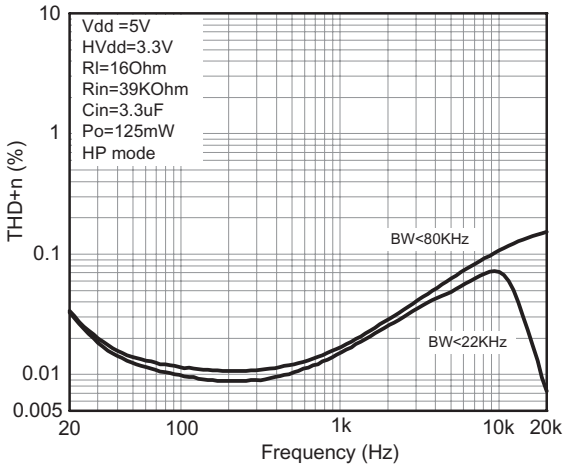


Figure 23. THD+n vs. Frequency

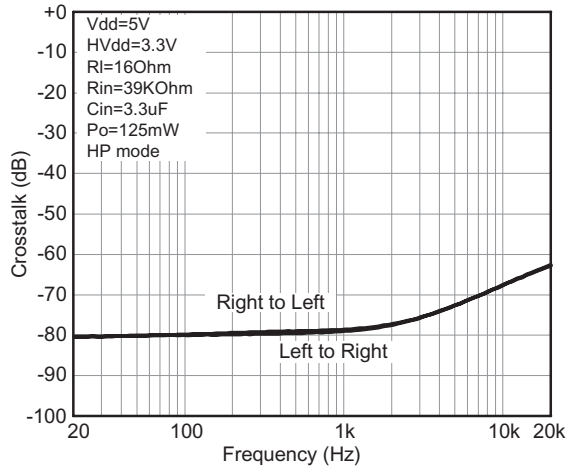


Figure 24. Crosstalk vs. Frequency

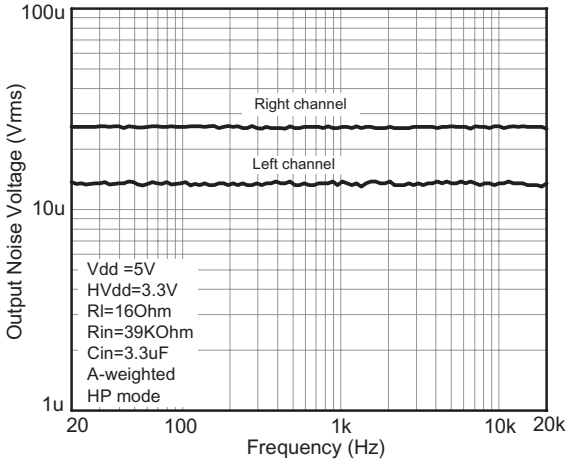


Figure 25. Output Noise Voltage vs. Frequency

Typical Operating Characteristics (Continued)

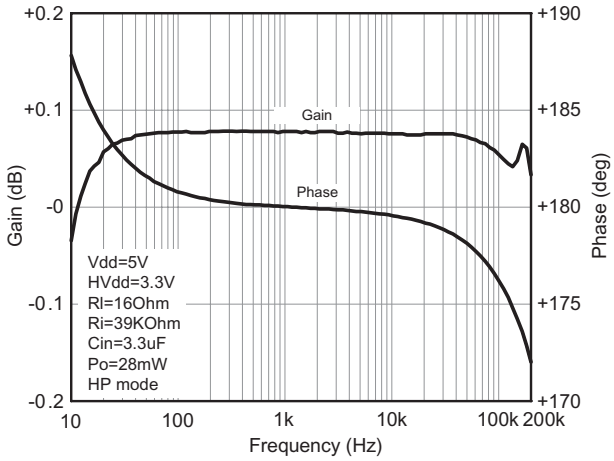


Figure 26. Frequency Response

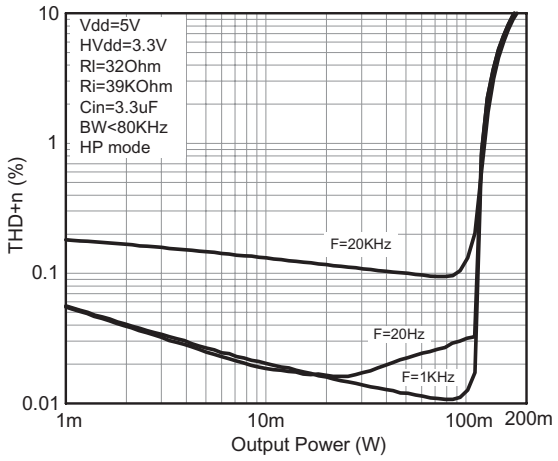


Figure 27. THD+N vs. Output Power

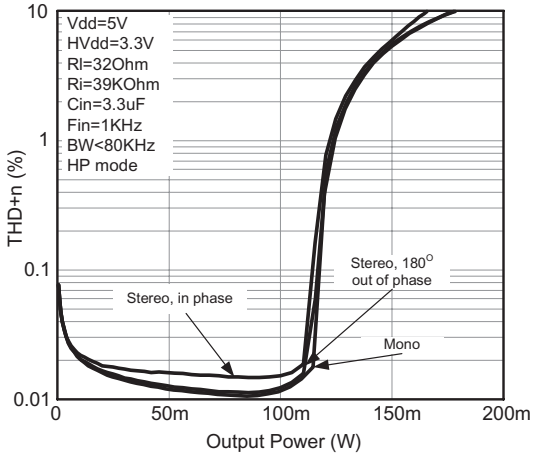


Figure 28. THD+N vs. Output Power

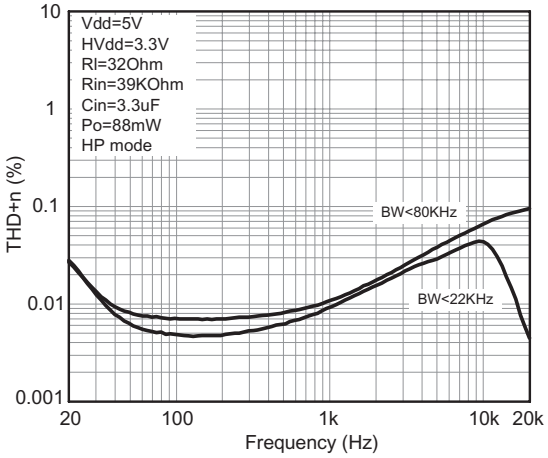


Figure 29. THD+n vs. Frequency

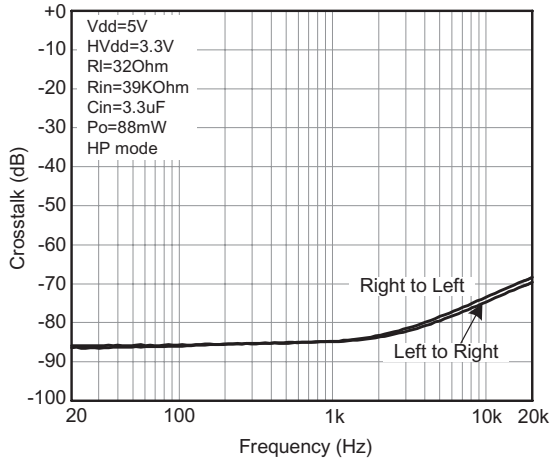


Figure 30. Crosstalk vs. Frequency

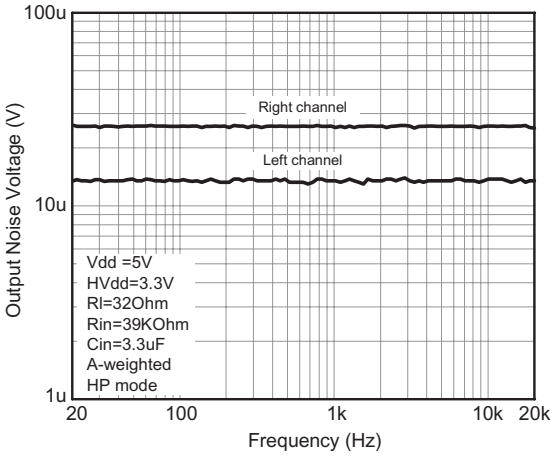


Figure 31. Output Noise Voltage vs. Frequency

Typical Operating Characteristics (Continued)

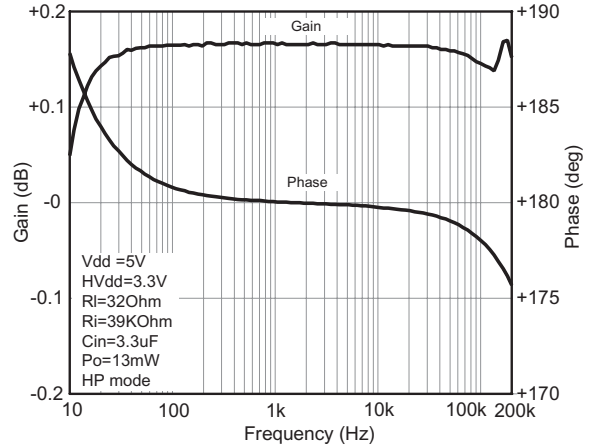


Figure 32. Frequency Response

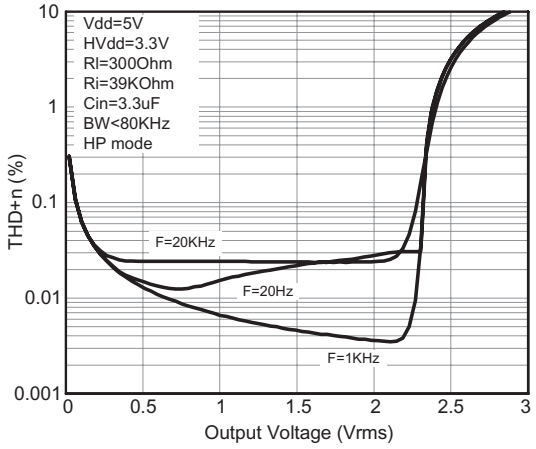


Figure 33. THD+n vs. Output Voltage

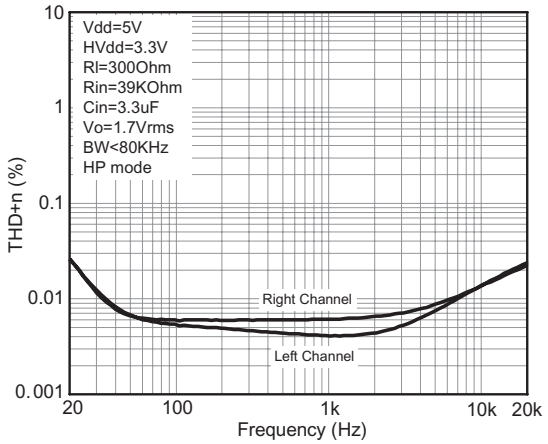


Figure 34. THD+n vs. Frequency

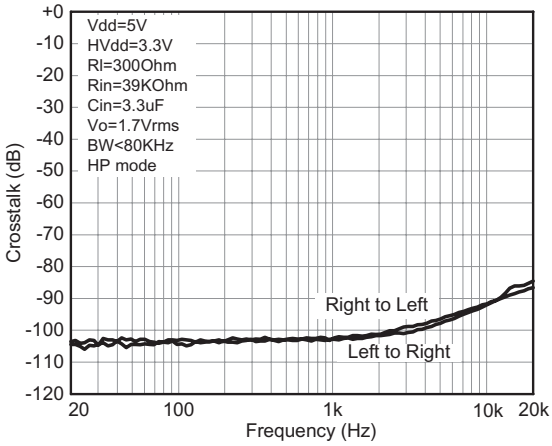


Figure 35. Crosstalk vs. Frequency

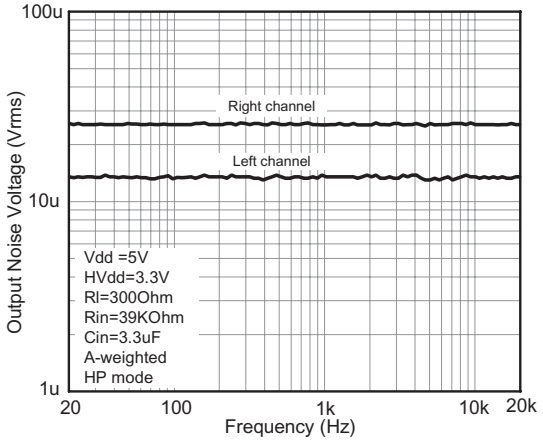


Figure 36. Output Noise Voltage vs. Frequency

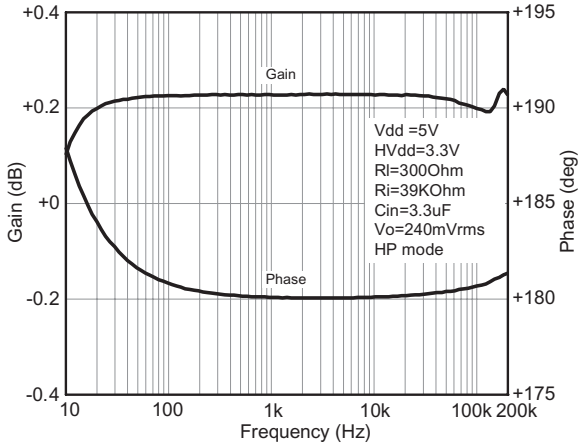


Figure 37. Frequency Response

Typical Operating Characteristics (Continued)

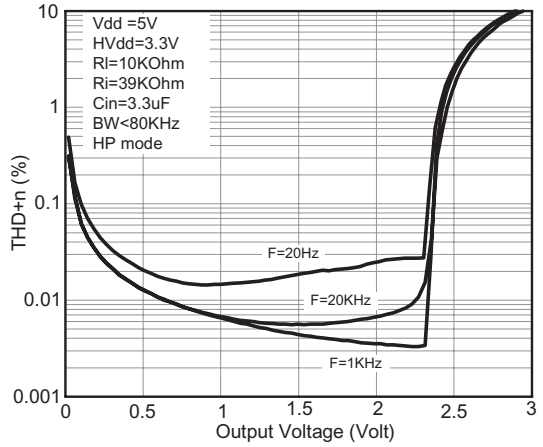


Figure 38. THD+n vs. Output Voltage

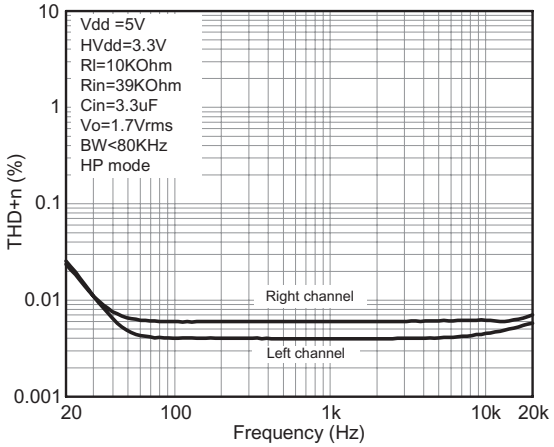


Figure 39. THD+n vs. Frequency

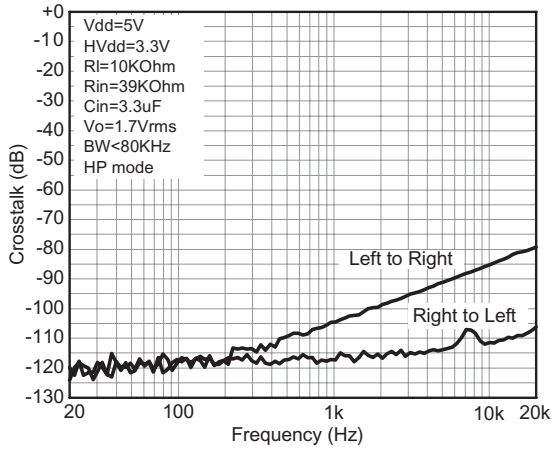


Figure 40. Crosstalk vs. Frequency

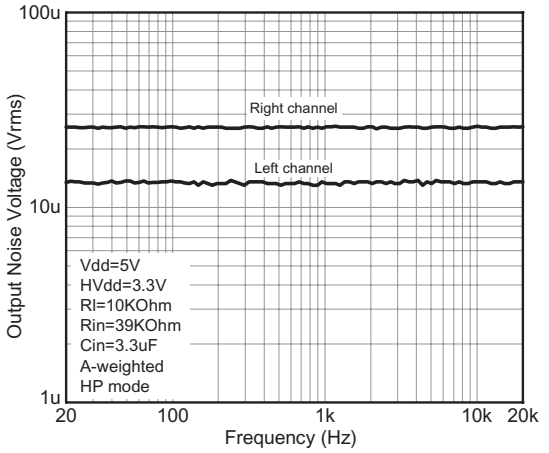


Figure 41. Output Noise Voltage vs. Frequency

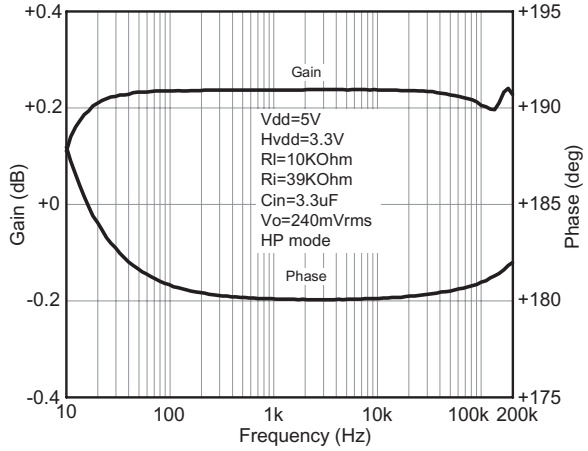


Figure 42. Frequency Response

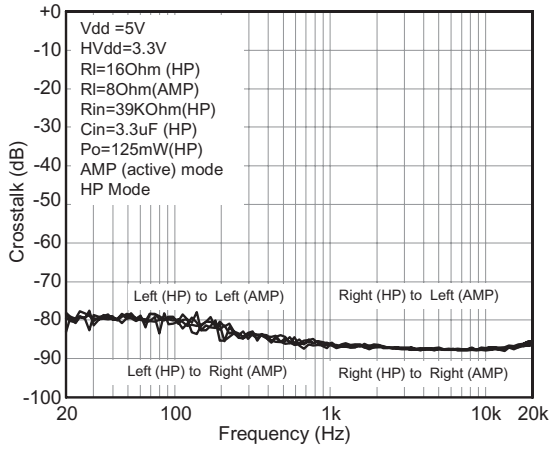


Figure 43. Crosstalk vs. Frequency

Typical Operating Characteristics (Continued)

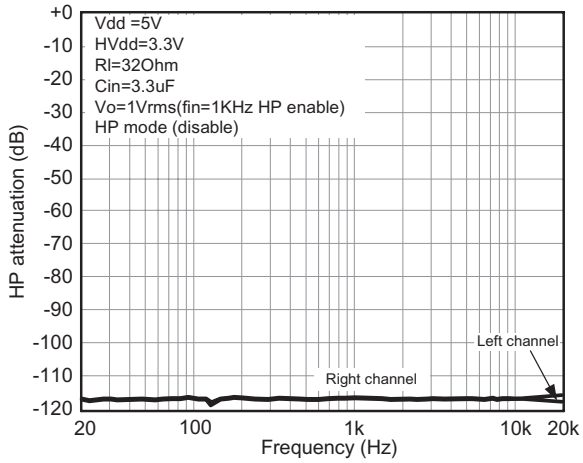


Figure 44. HP Attenuation vs. Frequency

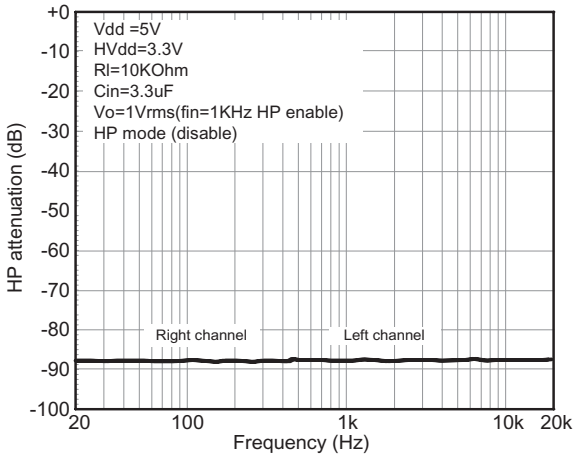


Figure 45. HP Attenuation vs. Frequency

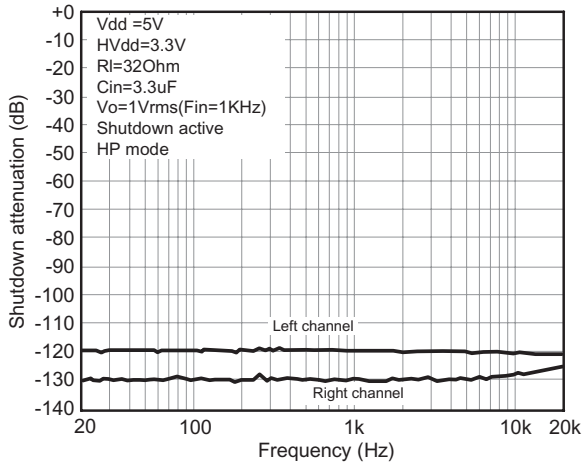


Figure 46. Shutdown Attenuation vs. Frequency

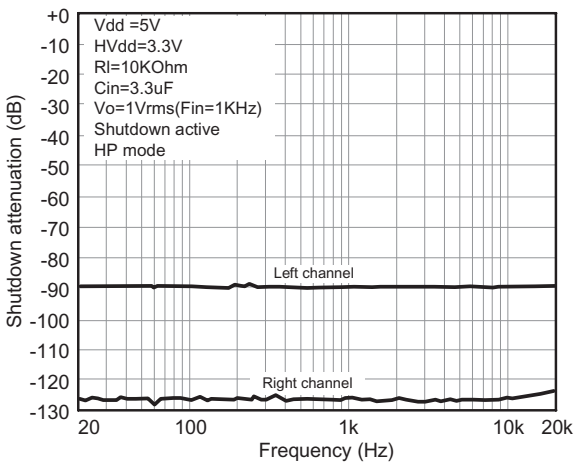


Figure 47. Shutdown Attenuation vs. Frequency

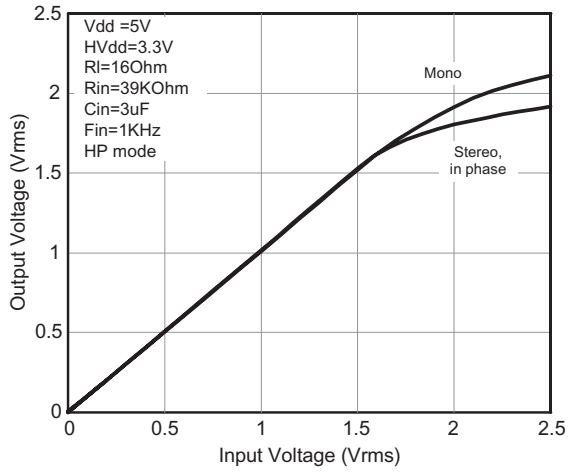


Figure 48. Input Voltage vs. Output Voltage

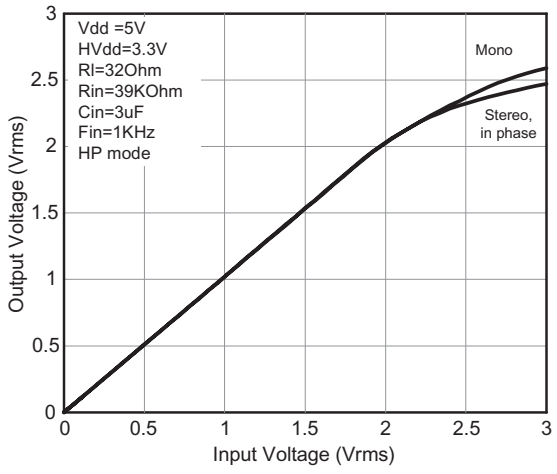


Figure 49. Input Voltage vs. Output Voltage

Typical Operating Characteristics (Continued)

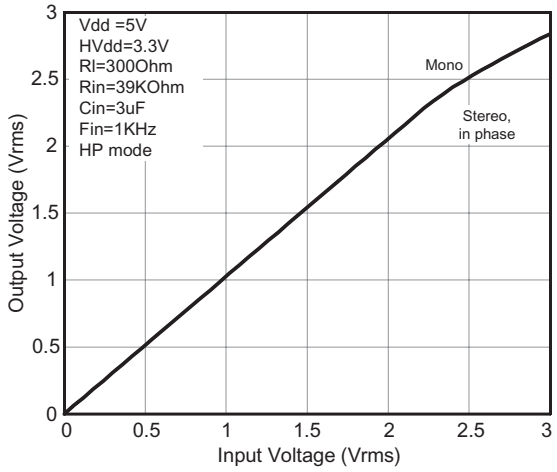


Figure 50. Input Voltage vs. Output Voltage

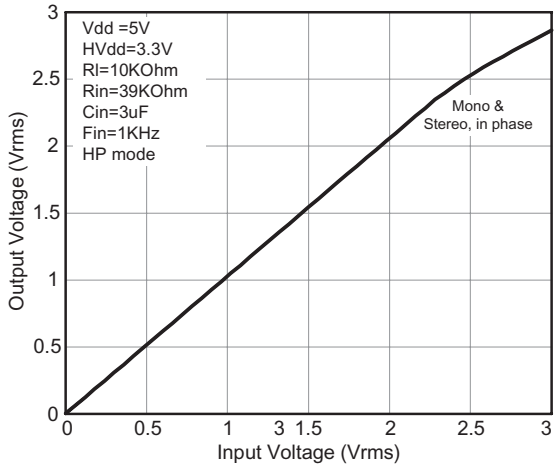


Figure 51. Input Voltage vs. Output Voltage

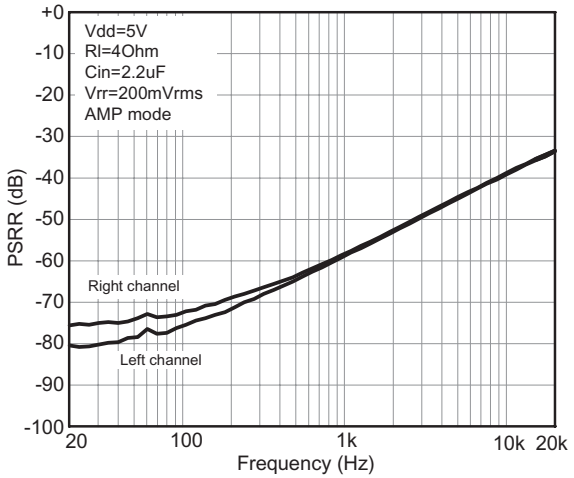


Figure 52. PSRR vs. Frequency

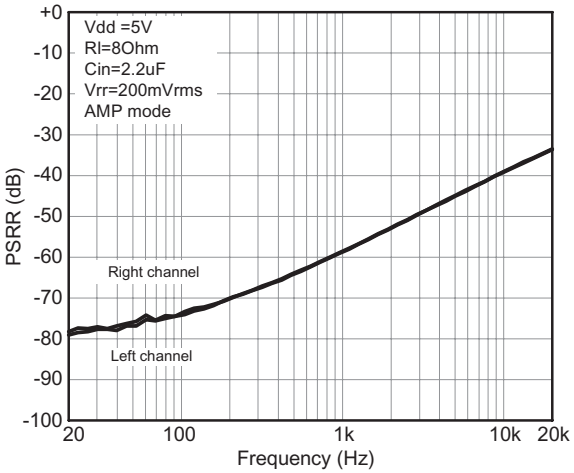


Figure 53. PSRR vs. Frequency

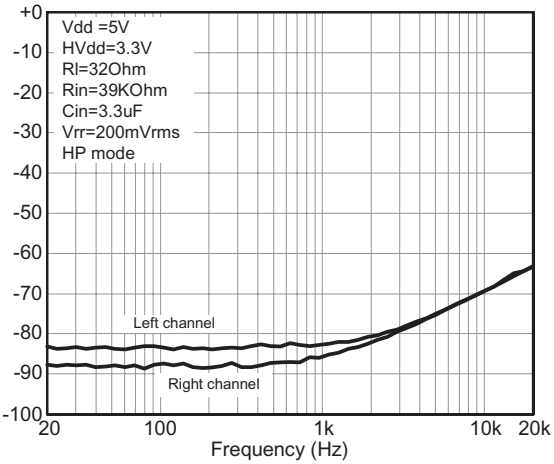


Figure 54. PSRR vs. Frequency

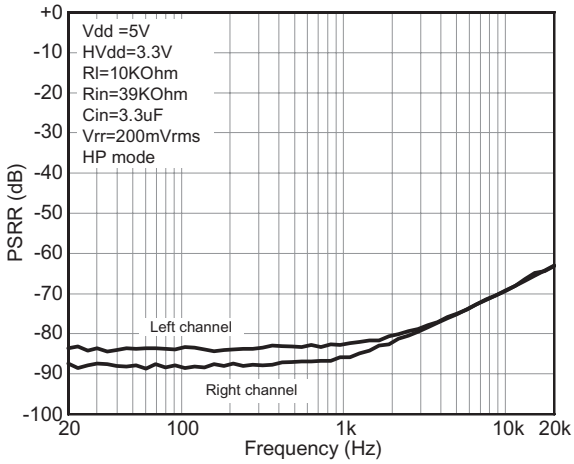


Figure 55. PSRR vs. Frequency

Typical Operating Characteristics (Continued)

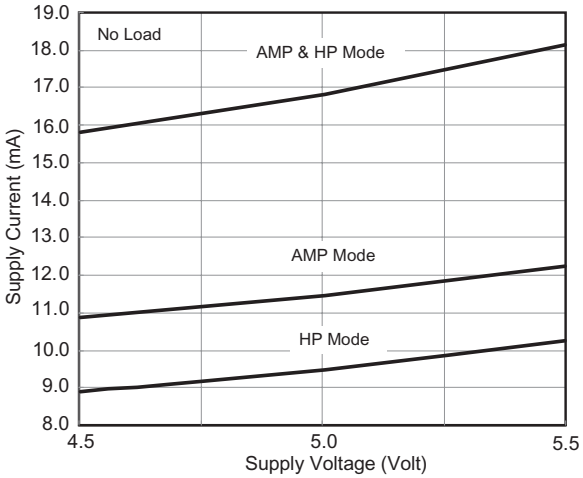


Figure 56. Supply Current vs. Supply Voltage

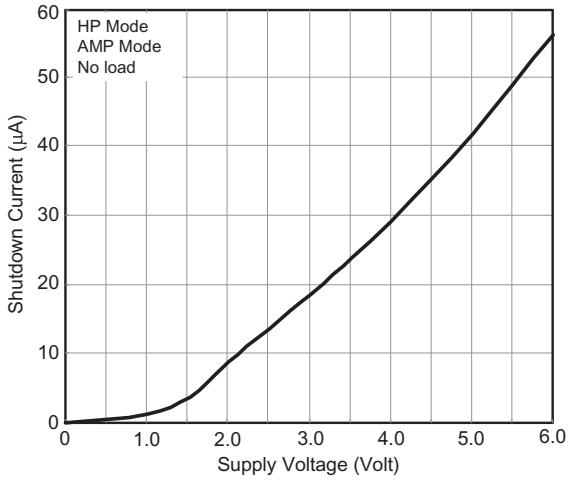


Figure 57. Supply Current vs. Supply Voltage

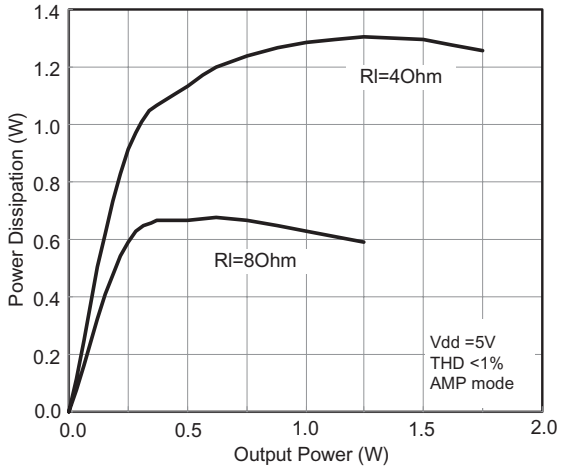


Figure 58. Power Dissipation vs. Output Power

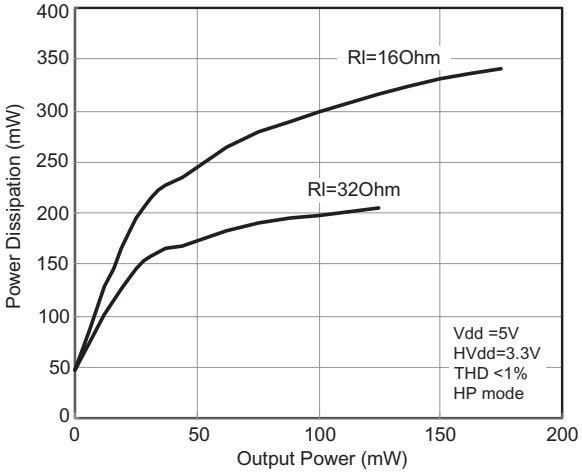


Figure 59. Power Dissipation vs. Output Power

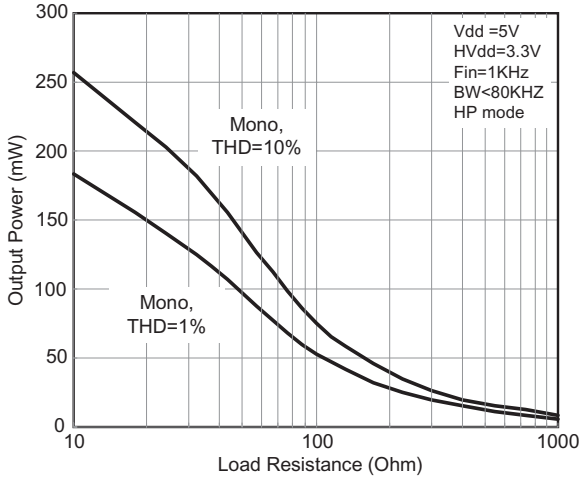


Figure 60. Output Power vs. Load Resistance

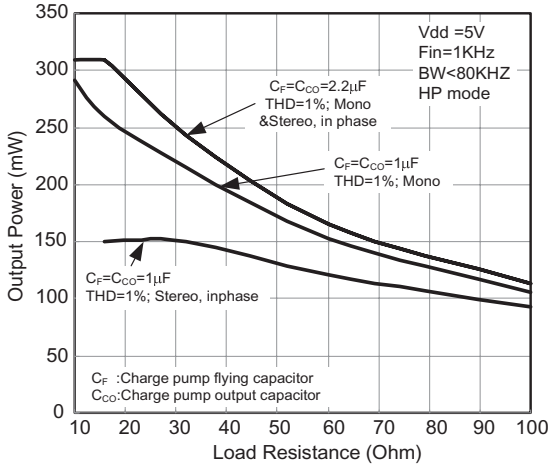


Figure 61. Output Power vs. Load Resistance and Charge Pump Capacitance

Typical Operating Characteristics (Continued)

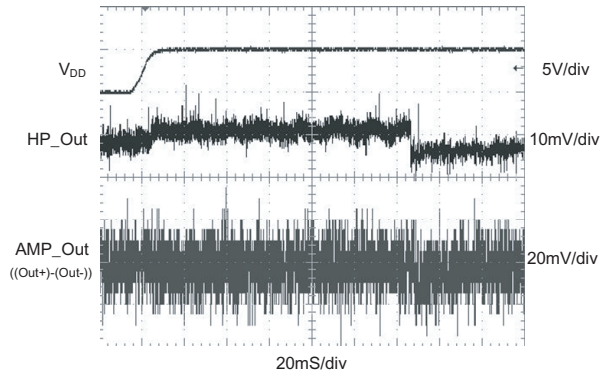


Figure 62. Output Transient at Turn On

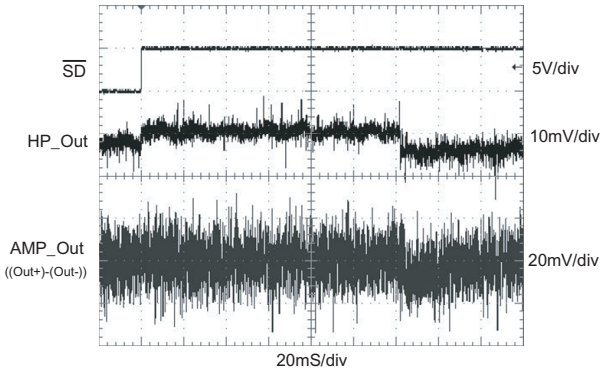


Figure 63. Output Transient at Shutdown Release

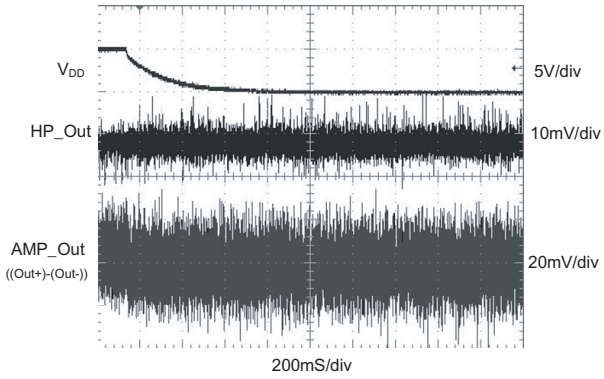


Figure 64. Output Transient at Turn Off

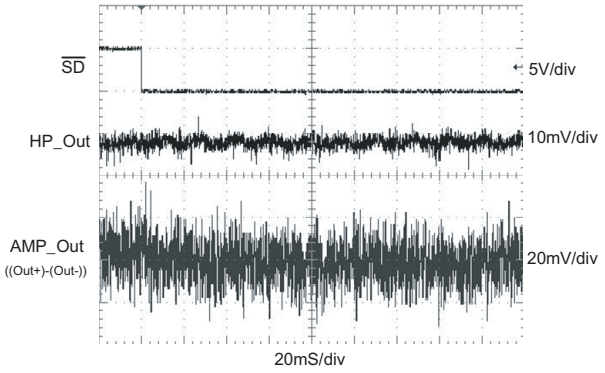
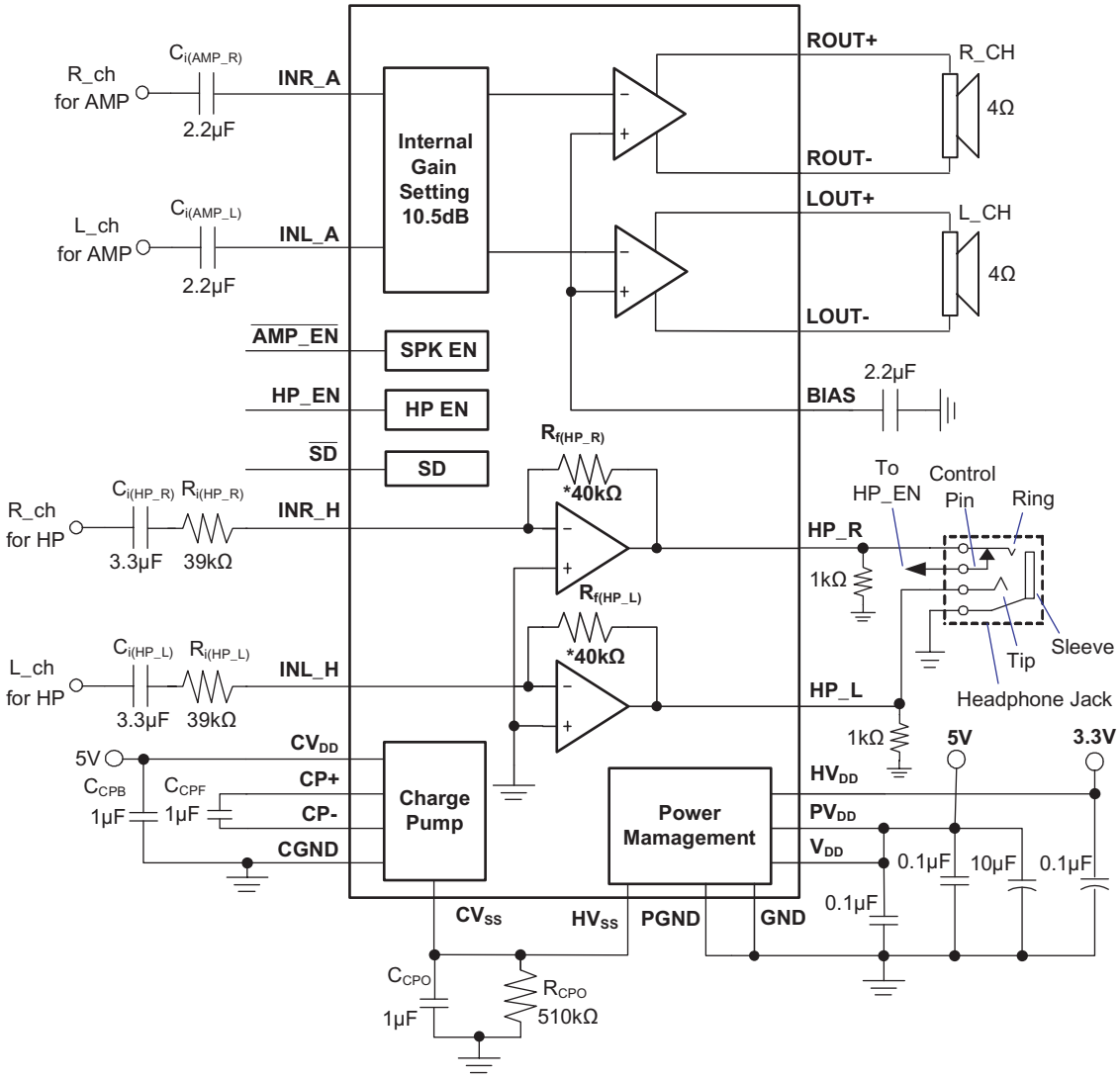


Figure 65. Output Transient at Shutdown Active

Typical Application Circuit



* The internal Rf's value has 10% variation by process

Figure 66.

Application Information

Amplifier Mode Operation

The FPA6101 has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

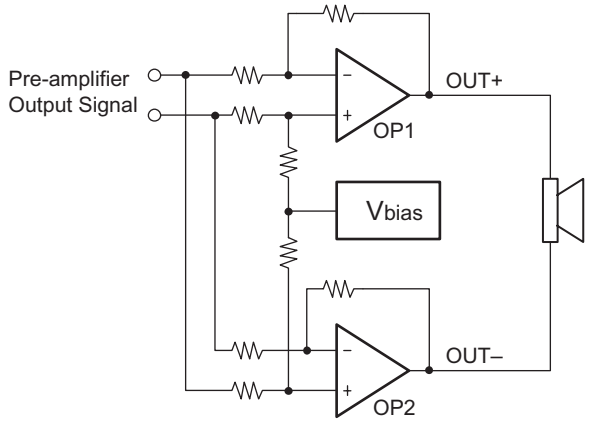


Figure 67. FPA6101 Internal Configuration (each channel)

The OP1 and OP2 are all differential drive configuration, The differential drive configuration doubling the voltage swing on the load compare to the single-ending configuration, the differential gain for each channel is 2x (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage. Four times the output power is possible as compared to a SE amplifier under the same conditions. A BTL configuration, such as the one used in FPA6101, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Headphone Mode Operation

The FPA6101's headphone amplifiers using a charge pump to invert the positive power supply (CV_{DD}) to negative power supply (CV_{SS}), see Figure 68. The headphone amplifiers operate at this bipolar power supply, and the outputs reference is refer to the ground. This feature eliminates the output capacitor that using in conventional single-ended headphone amplifier. Headphone amplifier internal supply voltage is come from HV_{DD} and V_{SC}. For good AC performance, the HV_{DD} connected to 3.3V is recommended. And it can be avoid the output voltage too big for line out application.

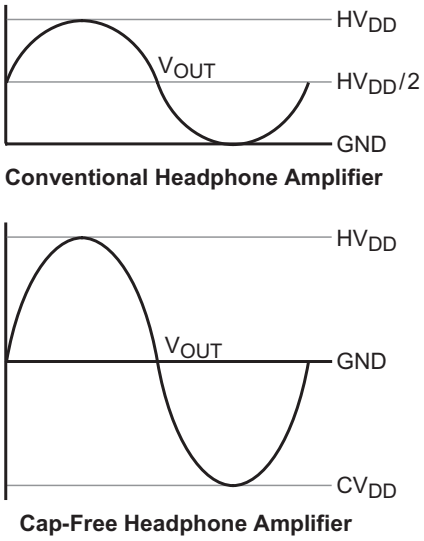


Figure 68. Cap-Free Operation

Charge Pump Flying Capacitor

The flying capacitor (C_{CPF}) affects the load transient of the charge pump. If the capacitor's value is too small that will degrade the charge pump's current driver capability, and degrade the performance of headphone amplifier.

Increasing the flying capacitor's value will improve the load transient of charge pump. Recommend using the low ESR ceramic capacitors (X7R type is Recommended) above 1µF.

Charge Pump Output Capacitor

The output capacitor (C_{CPO})'s value affects the power ripple directly at CV_{SS} (V_{SS}). Increasing the value of output capacitor reduces the power ripple. The ESR of output capacitor affects the load transient of CV_{SS} (V_{SS}). Low ESR and greater than 1µF ceramic capacitor (X7R type is suggested) is recommended.

Charge Pump Bypass Capacitor

The bypass capacitor (C_{CPB}) relate with the charge pump switching transient. The capacitor's value is same as flying capacitor (1µF) Place it close to the CV_{DD} and PGND.

Headphone Detection Input

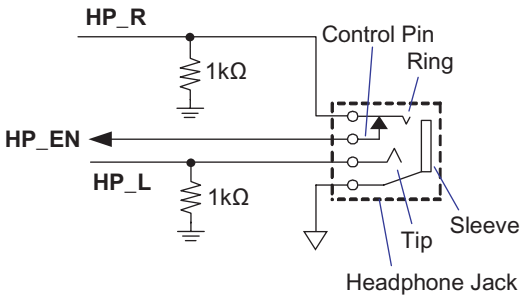


Figure 69. HPD Configurations

The HP_EN detect the voltage, less than 0.8V it disable headphone amplifiers; greater than 2V, enable the headphone amplifier.

In Figure 69, using a phone-jack that has control pin, and connect the control pin to HP_EN input. When a headphone plug is inserted, the HP_EN will pull high by internal then enable headphone amplifiers; without headphone plug the HP_EN is pull to GND.

Operation Mode

FPA6101 amplifier has two pairs independent amplifier, one for stereo speaker is a BTL structure, and the other for headphone is cap-less structure. And each pair have independent input pin, INR_A and INA_L are for stereo speaker drivers, INR_H and INL_H are for stereo headphone drivers.

Amplifier mode operation: Pull low the AMP_EN control pin can enable the stereo speaker driver.

Headphone mode operation: Pull high the HP_EN control pin can enable the cap-less headphone drive.

Both amplifier and headphone "ON" mode: Pull low the AMP_EN and pull high the HP_EN control pins, will turn on both speaker drivers and headphone drivers

Both amplifier and headphone "OFF" mode: Pull high the AMP_EN and pull low the HP_EN control pins, will turn off both speaker drivers and headphone drivers

If connect the AMP_EN and HP_EN together, then connect this pin to headphone jack's control pin (Figure 69), the FPA6101 can switch between the "Amplifier mode (Headphone mute), or Headphone mode (Amplifier mute).

Gain Setting

The gain for speaker driver is 10.5dB, but it can low down the gain by external input resistor (Ri.external). that add on INR_A and INL_A input pins. The Table 1 shows the reference gain setting with external input resistor (Ri. external) for speaker amplifier (AMP Mode).

For headphone driver, the internal feedback resistor is 40kW ($R_{f(HP)}$ external, 10% variation by process), so the headphone driver's gain is setting by the input resistor ($R_{i(HP)}$ external), Table 1 show the reference gain setting with external resistor for headphone driver (HP Mode).

Input Capacitor, Ci

In the typical application an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form a high-pass filter with the corner frequency determined in the follow equation:

$$f_C \text{ (highpass)} = 1 / (2\pi Ri(min) \bullet Ci) \quad (1)$$

Table 1. Gain Settings

Amp Mode (10.dB default gain)			
R_i,external (kΩ)	**OUTP (V/V)**	**BTL O/P (V/V)**	**Gain (dB)**
6.2	1.25	2.51	8.0
3.3	1.42	2.85	9.1
1	1.59	3.19	10.1
0	1.68	3.36	10.5
HP Mode			
$R_{i(HP)}$,external (kΩ)	**$R_{i(HP)}$,internal (kΩ)**	**HP OUT (V/V)**	**HP Gain (dB)**
62	40	0.65	-3.8
50	40	0.80	-1.9
39	40	1.03	0.2
30	40	1.33	2.5
24	40	1.67	4.4
20	40	2.00	6.0

*The internal Rf's value has 10% variation by process.

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where Ri is 10kΩ and the specification calls for a flat bass response down to 10Hz. Equation is reconfigured as follow:

$$Ci = \frac{1}{2\pi RiF_C} \quad (2)$$

Consider to input resistance variation, the Ci is 1.6 so one would likely choose a value in the range of 2.2μF to 3.3μF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ri + Rf, Ci) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at $V_{DD}/2$, which is likely higher that the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bias Capacitor, Cbypass

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger bypass capacitor is improved PSRR due to increased 1.8V bias voltage stability. Typical applications employ a 5V regulator with 2.2μF and a

0.1µF bypass capacitor, which aid in supply filtering. This does not eliminate the need for bypassing the supply nodes of the FPA6101. The selection of bypass capacitors, especially Cb, is thus dependent upon desired PSRR requirements, click and pop performance.

Power Supply Decoupling, Cs

The FPA6101 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best (the pin 1 (V_{DD}) and pin 2 (GND)'s capacitor must short less than 1cm). For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Shutdown Function

In order to reduce power consumption while not in use, the FPA6101 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the SD pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between ground and the supply V_{DD} to provide maximum device performance.

By switching the SD pin to low, the amplifier enters a low-current state, I_{DD} < 80µA. FPA6101 is in shutdown mode, except PC-BEEP detects circuit. On normal operating, SD pin pull to high level to keeping the IC out of the shutdown mode. The SD pin should be tied to a definite voltage to avoid unwanted state changes. The wake-up time of shutdown is about 150mS, and the shutdown release's pop is cause by the operational amplifier's offset.

PC-BEEP Detection

FPA6101 integrates a PCBEEP detect circuit for NOTEBOOK PC used. When PC-BEEP signal drive to PCBEEP input pin, and PCBEEP mode is active. FPA6101 will turn on speaker drivers and the internal gain fixed as 0dB. The PCBEEP signal becomes the amplifiers input signal. If the amplifiers in the shutdown mode, it will out of shutdown mode whenever PCBEEP mode enable. The FPA6101 will return to previous setting when it is out of PC BEEP mode.

The input impedance is 100kΩ on PCBEEP input pin.

Speaker Driver Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{Psup} \quad (3)$$

where,

$$P_O = \frac{V_O rms \bullet V_O rms}{R_L} = \frac{(V_P \bullet V_P)}{2R_L} \quad (4)$$

$$V_O rms = \frac{V_P}{\sqrt{2}} \quad (5)$$

$$Psup = V_{DD} \bullet I_{DD}(AVG) = V_{DD} \bullet \frac{2V_P}{\pi R_L} \quad (6)$$

Efficiency of a Differential configuration:

$$\frac{P_O}{Psup} = \left\{\frac{(V_P \bullet V_P)}{2R_L}\right\} \Big/ \left\{V_{DD} \bullet \frac{2V_P}{\pi R_L}\right\} = \frac{\pi R_L}{4V_{DD}} \quad (7)$$

Table 2 calculates efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8W loads and a 5V supply, the maximum draw on the power supply is almost 3W.

Table 2. Efficiency vs. Output Power in 5V/8W Differential Amplifier Systems

P_O (W)	Efficiency (%)	I_{DD} (A)	V_{PP} (V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

*High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation 8 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE Mode: } P_{D,MAX} = \frac{V_{DD}^2}{2\pi R_L} \quad (8)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL Mode: } P_{D,MAX} = \frac{4V_{DD}^2}{2p^2 R_L} \quad (9)$$

Since the FPA6101 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the FPA6101 does not require extra heatsink. The power dissipation from equation 9, assuming a 5V power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation 9:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (10)$$

For TSSOP-28 packages with thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of FPA6101 is 150°C and the ambient temperature (TA) is defined by the power system design, the maximum power dissipation that the IC package is able to handle can be obtained from equation 10. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the FPA6101 requires special attention on thermal design. If the thermal design issues are not properly addressed, the FPA6101 4Ω will go into thermal shutdown when driving a 4Ω load. The thermal pad on the bottom of the FPA6101 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 15 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the FPA6101 junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown. See Demo Board Circuit Layout as an example foe PCB layout.

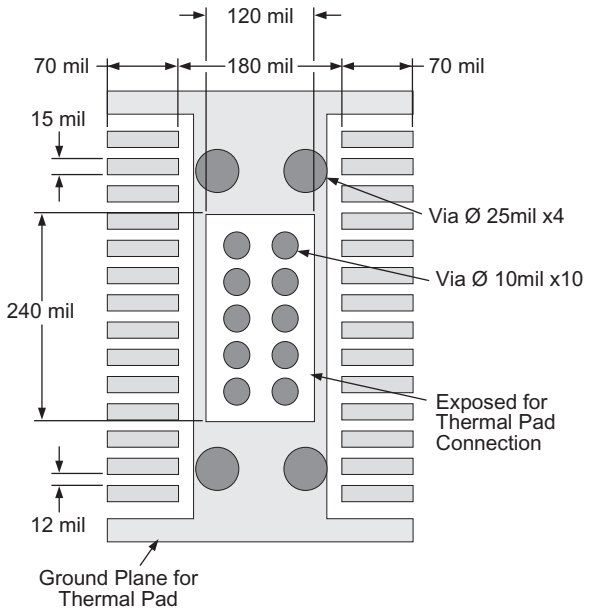


Figure 70. TSSOP28 Layout Recommendations

Thermal Considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. In the Power Dissipation vs. Output Power graph, the FPA6101 is operating at a 5V supply and a 4Ω speaker that 2W output power peaks are available. The vertical axis gives the information of power dissipation (P_D) in the IC with respect to each output driving power (P_O) on the horizontal axis.

This is valuable information when attempting to estimate the heat dissipation of the IC requirements for the amplifier system.

Using the power dissipation curves for a 5V/4Ω system, the internal dissipation in the FPA6101 and maximum ambient temperatures is shown in Table 3.

Table 3. FPA6101 Power Information, 5V/4Ω, Stereo, Differential Mode

Peak Output Power (W)	Average Output Power (W)	Power Dissipation (W/Channel)	Max. T_A with Thermal Pad (°C)
2	1.95	1.25	37
2	1.17	1.25	37
2	0.74	1.19	43
2	0.43	1.05	55
2	0.19	0.8	78

Table 4. Thermal Resistance

Package	θ_{JA}
TSSOP 28	45°C/W
MLP	TBD°C/W

This parameter is measured with the recommended copper heat sink pattern on a 2-layer PCB, 23cm^2 in 5.7mm x 4mm in PCB, 2oz. Copper, 100mm^2 coverage. Airflow 0 CFM The maximum ambient temperature depends on the heat sink ability of the PCB system.

To calculate maximum ambient temperatures, first consideration is that the numbers from the dissipation graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation.

Given θ_{JA}, the maximum allowable junction temperature. ($T_{J,Max}$), and the total antimale dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the FPA6101 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs. Output Power graph.

$$T_{A,MAX} = T_{J,MAX} - \theta_{JA} P_D \quad (11)$$

150 – 45(0.8 • 2) = 78°C (with Thermal Pad)

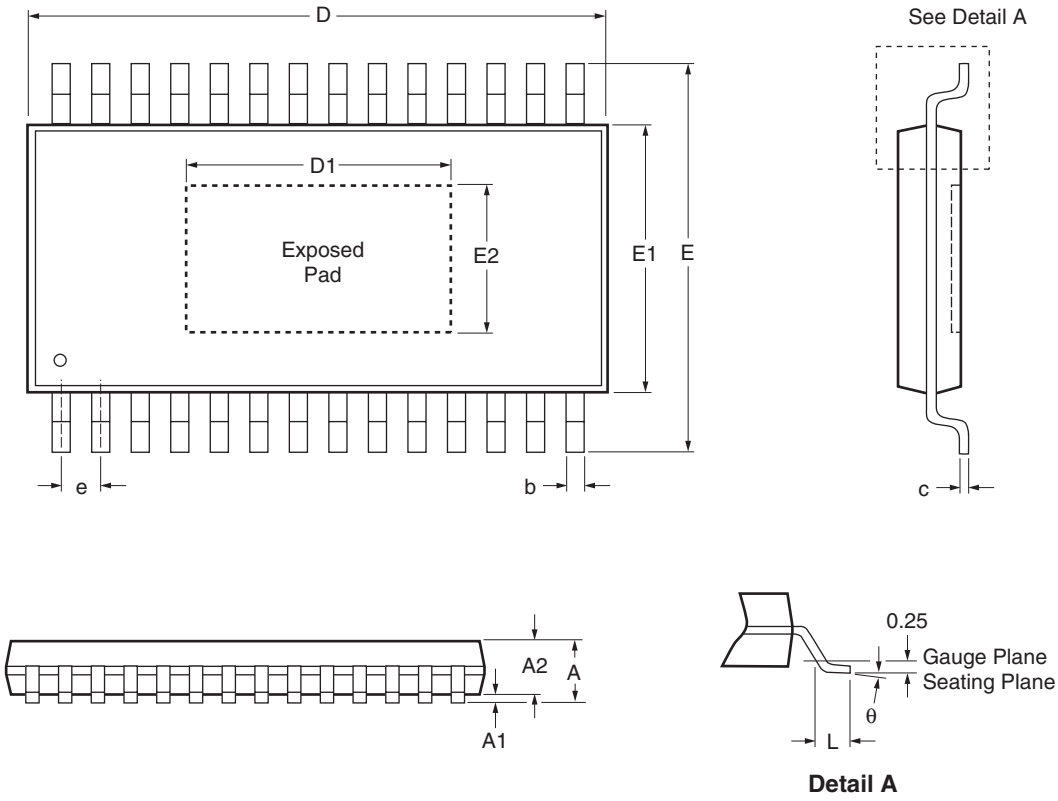
Note:

5. Internal dissipation of 0.8W is estimated for a 2W system with 15dB headroom per channel.

Table 3 shows that for some applications no airflow is required to keep junction temperatures in the specified range. The FPA6101 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC. The information in Table 3 was calculated for maximum listen volume with limited distortion. When the output level is reduced, the numbers in the table change significantly. Also, using 8Ω speakers will dramatically increase the thermal performance by increasing amplifier efficiency.

Packaging Dimensions

TSSOP-28

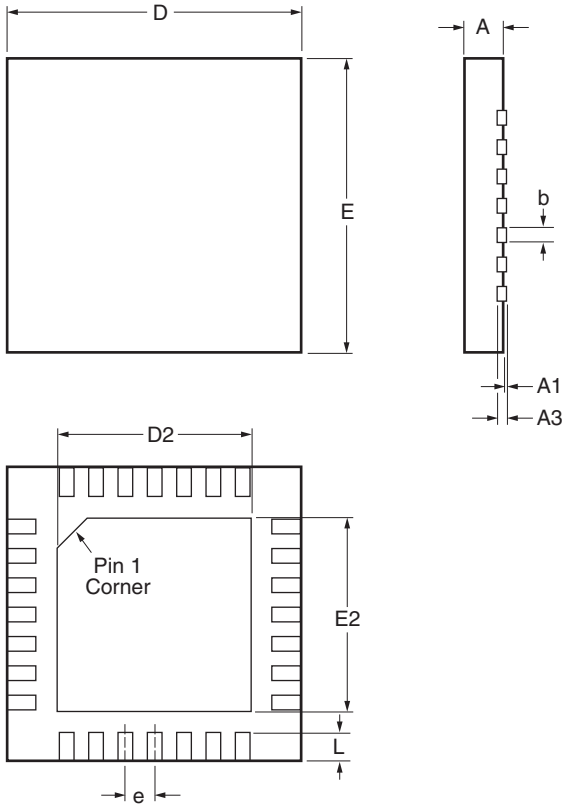


Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
D1	3.30		0.130	
E	6.40 BSC		6.40 BSC	
E1	4.30	4.50	0.169	0.177
E2	1.50		0.059	
e	0.65 BSC		0.65 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Figure 71.

Packaging Dimensions (Continued)

MLP 5x5-28

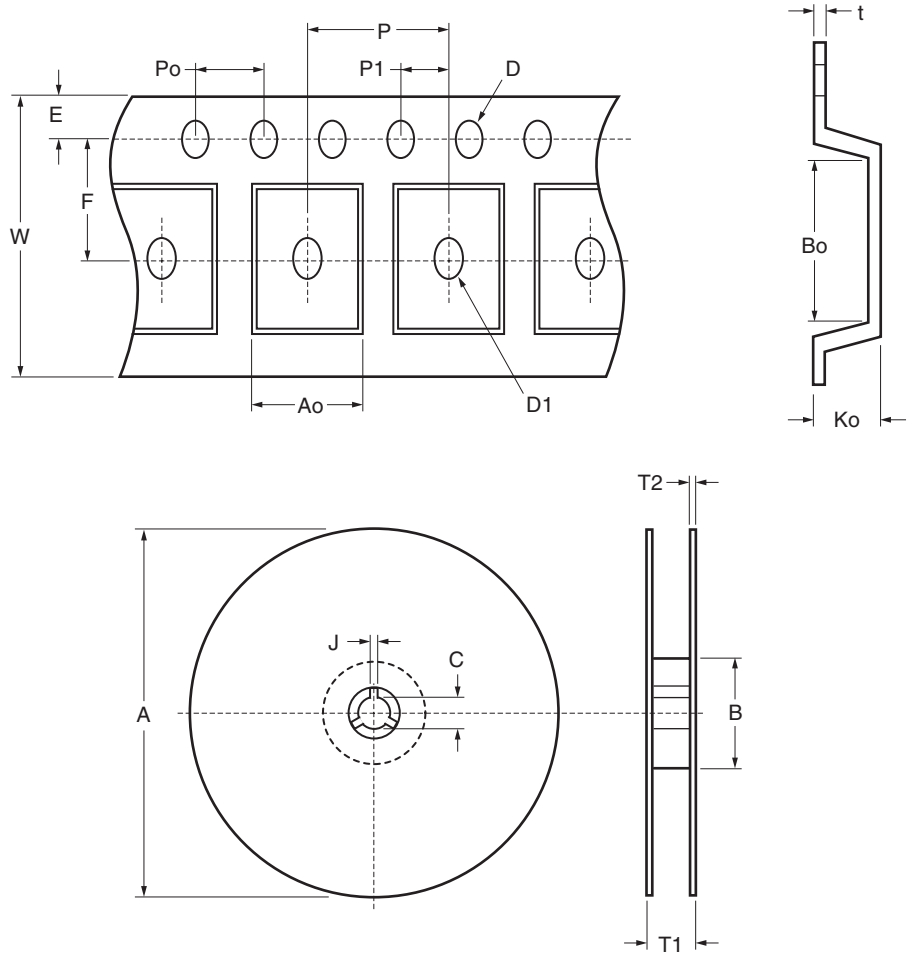


Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.197 BSC	
D2	3.50	3.80	0.138	0.150
E	5.00 BSC		0.197 BSC	
E2	3.50	3.80	0.138	0.150
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018

Figure 72.

Tape and Reel Dimensions

TSSOP-28P



A	B	C	J	T1	T2	W	P	E
330±1	100 ref.	13±0.5	2±0.5	16.4±0.2	2±0.2	16±0.3	12±0.1	1.75±0.1
F	**D**	**D1**	**Po**	**P1**	**Ao**	**Bo**	**Ko**	**t**
7.5±0.1	1.5±0.1	1.5 min.	4.0±0.1	2.0±0.1	6.9±0.1	10.2±0.1	1.8±0.1	0.3±0.05

Figure 73.

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices per Reel
TSSOP-28P	16	21.3	2000

5 x 5 Shipping Tray

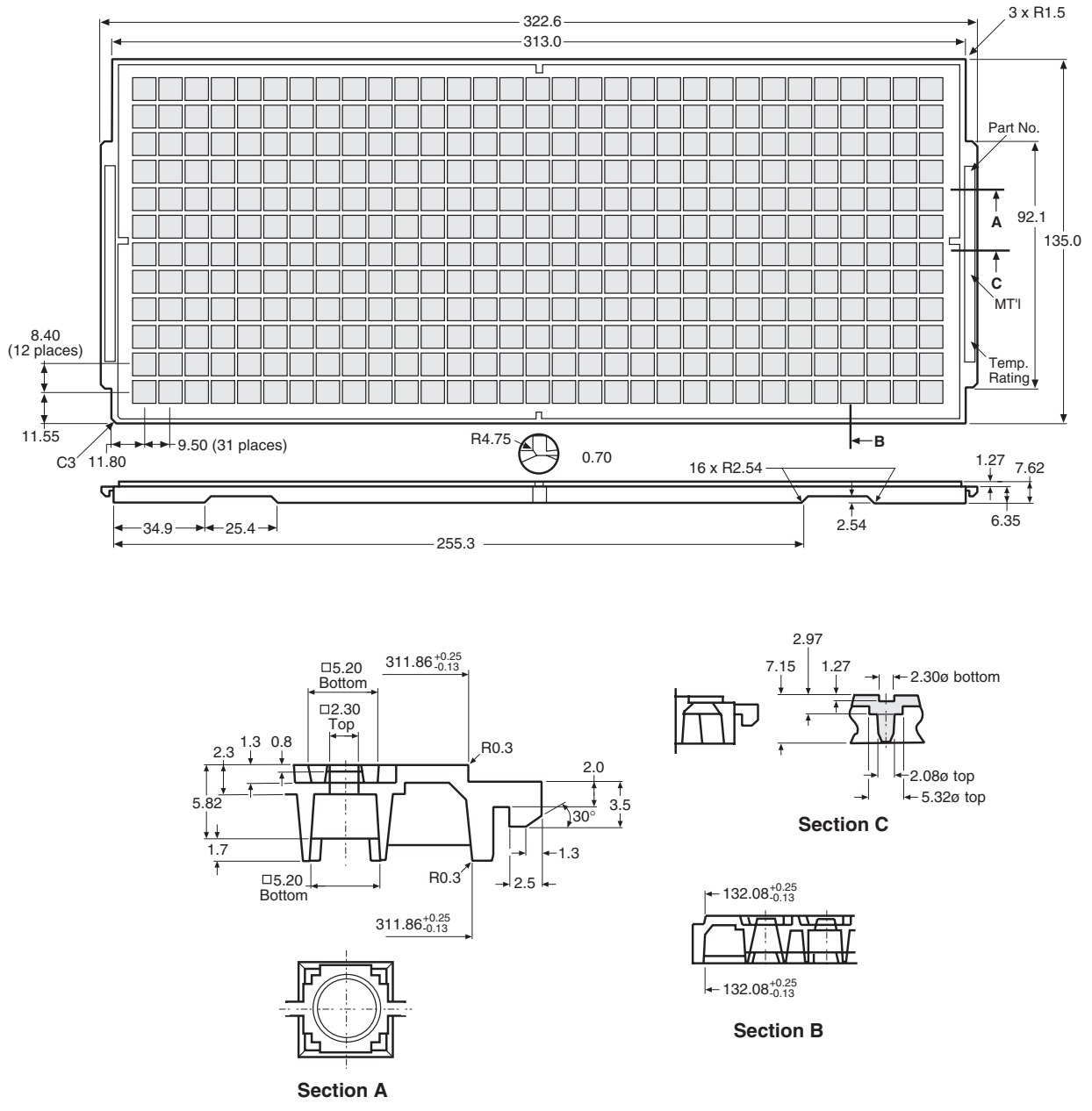


Figure 74.

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