

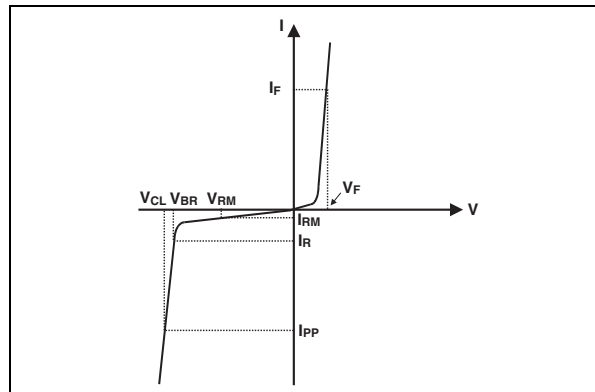
EMIF10-LCD01C2

Table 2: Absolute Maximum Ratings ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

Table 3: Electrical Characteristics ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
Cline	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1 \text{ mA}$	6	8	10	V
I_{RM}	$V_{RM} = 3\text{V}$			500	nA
$R_{I/O}$		90	100	110	Ω
Cline	@ 0V bias		28	35	pF
Rt / Ft	Induced rise and fall time 10-90% at 26 MHz frequency signal $V = 1.9 \text{ V}$ (Rt / Ft input 1 ns, 50 Ω impedance generator)		8 (1)		ns

(1) guaranteed by design

Figure 3: S21(dB) all lines attenuation measurement and ApIac simulation

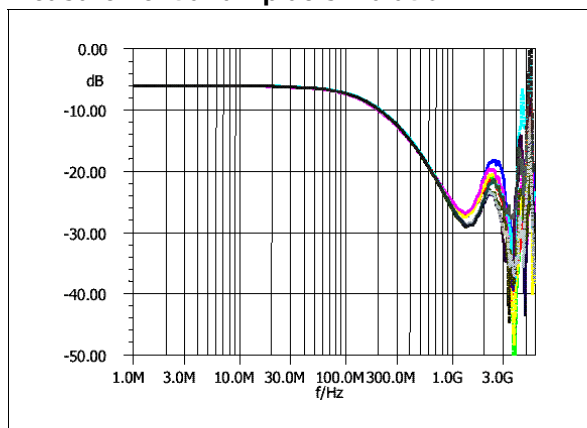


Figure 4: Analog cross talk measurements

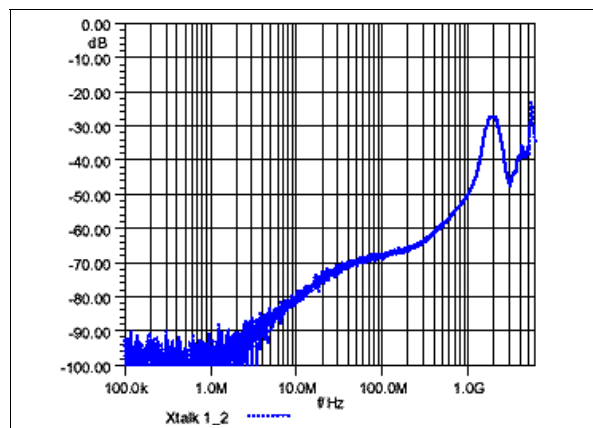


Figure 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input and on one output

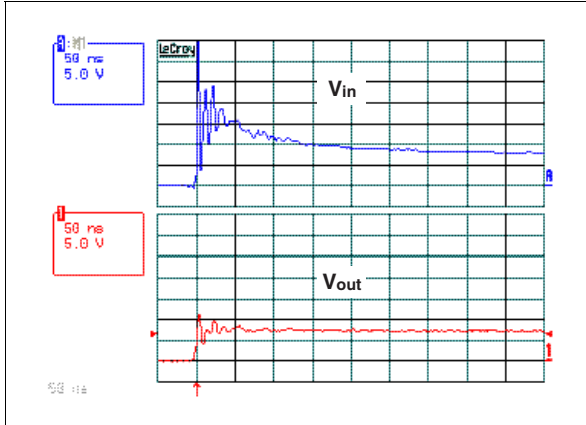


Figure 6: ESD response to IEC61000-4-2 (-15kV air discharge) on one input and on one output

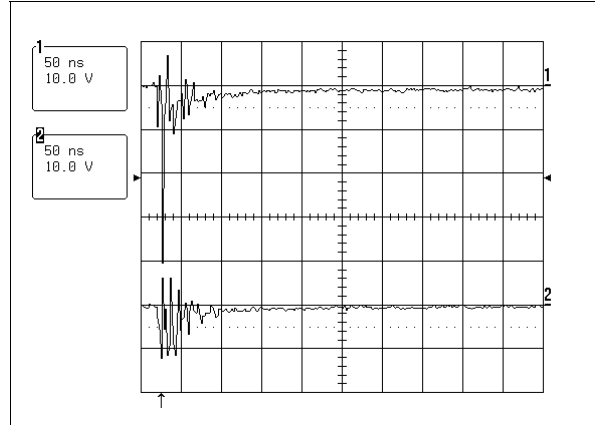


Figure 7: Line capacitance versus applied voltage

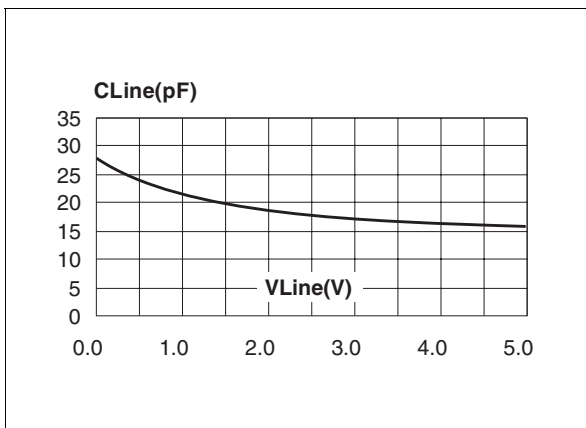


Figure 8: Rise time 10-90% measurements with 1.9V signal at 26 MHz frequency (50Ω generator)

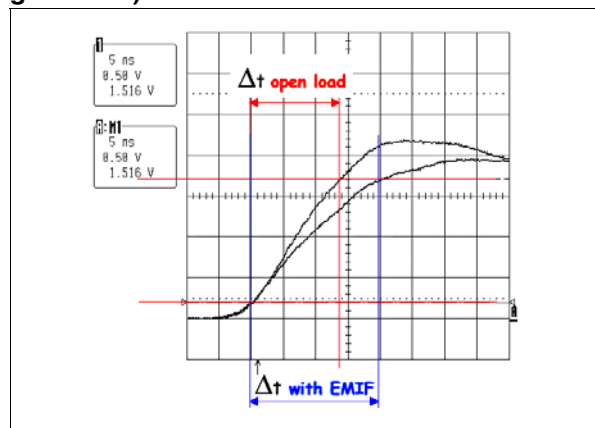


Figure 9: Fall time 10-90% measurements with 1.9V signal at 26 MHz frequency (50Ω generator)

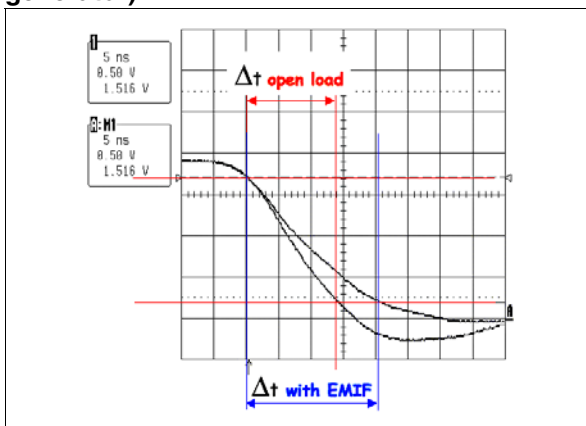


Figure 10: Aplac model

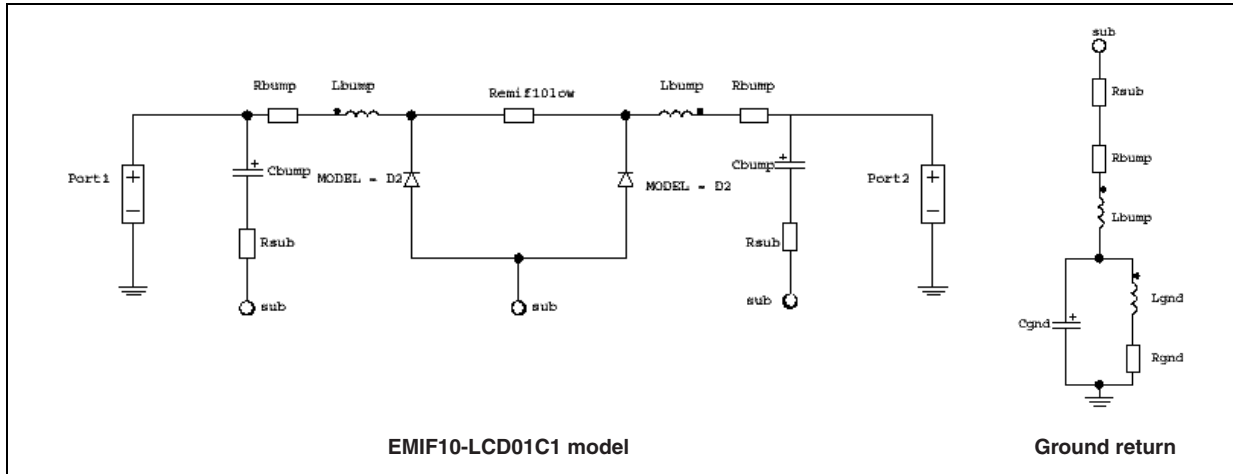


Figure 11: Aplac parameters

ZRZ structure	
aplacvar Remif10low 100	BV = 7
aplacvar Cemif10flow 17.5pF	CJO = Cemif10low
Bumps	IBV = 1u
aplacvar Lbump 50pH	IKF = 1000
aplacvar Rbump 20m	IS = 10f
aplacvar Cbump 1.5pF	ISR = 100p
Bulk	N = 1
aplacvar Rsub 100m	M = 0.3333
Gnd connections	RS = 0.015
aplacvar Rgnd 100m	VJ = 0.6
aplacvar Lgnd 200pH	TT = 50n
aplacvar Cgnd 0.15pF	

Figure 12: Order Code

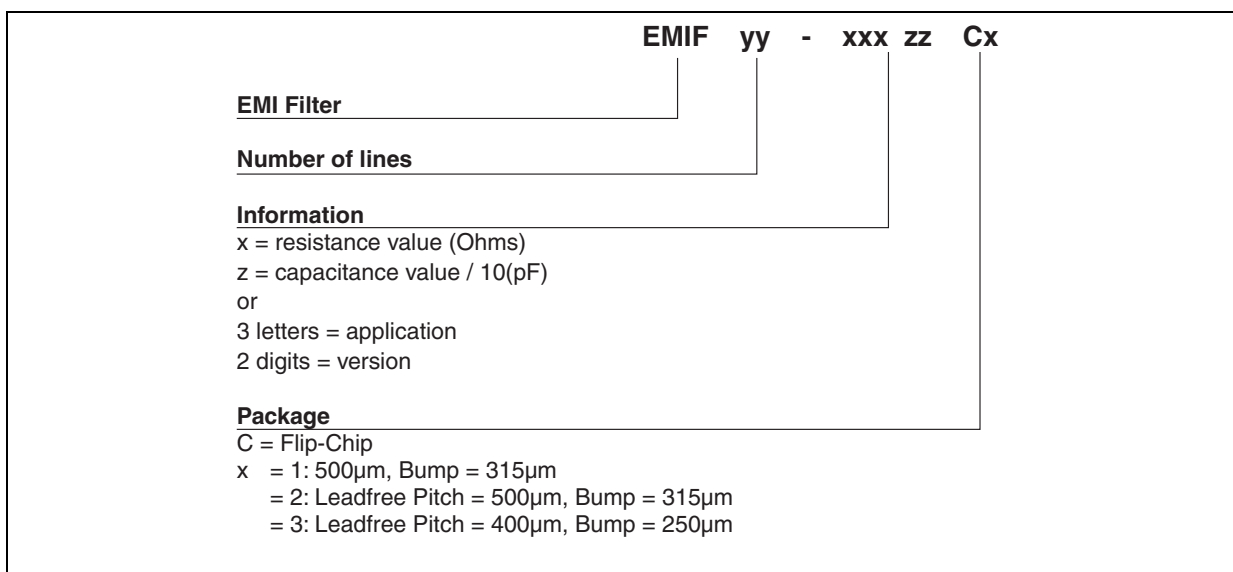


Figure 13: FLIP-CHIP Package Mechanical Data

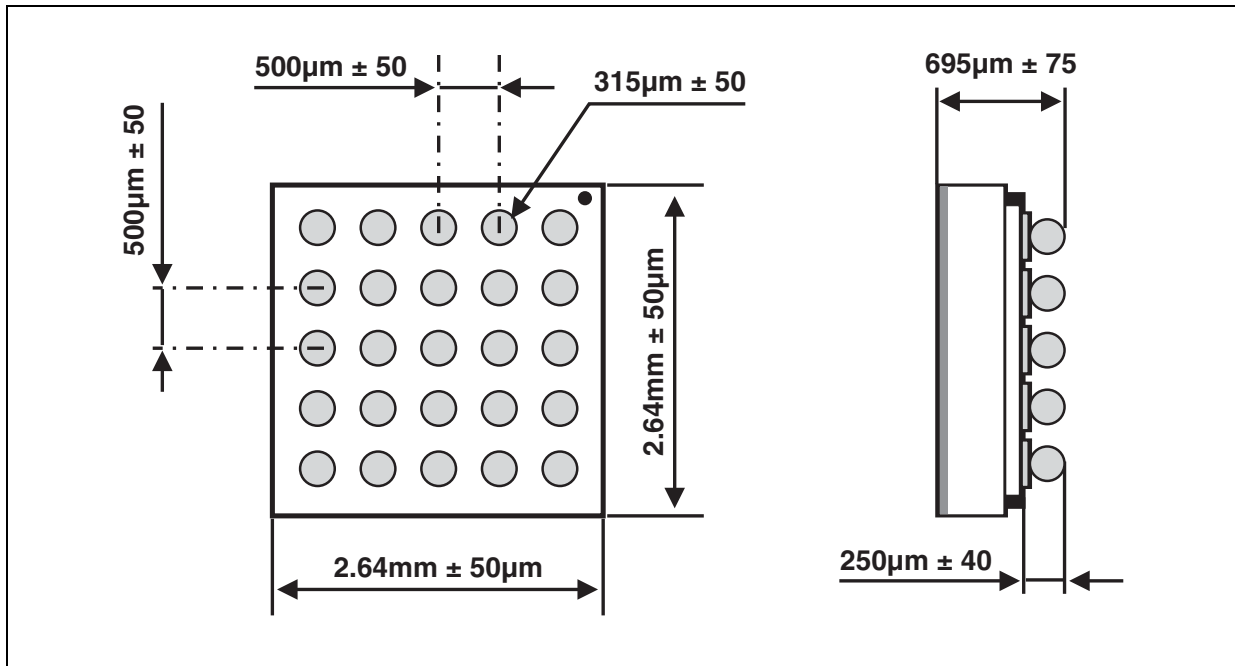


Figure 14: Foot Print Recommendations

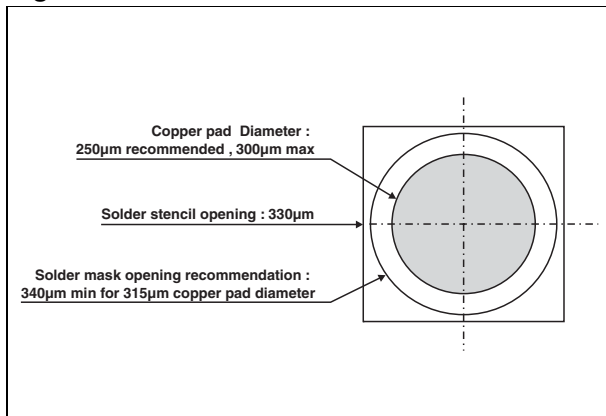


Figure 15: Marking

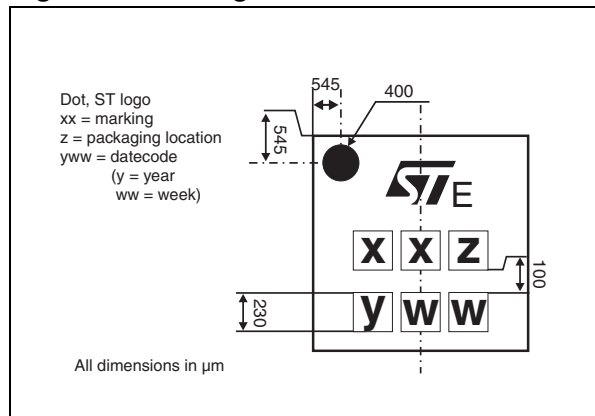
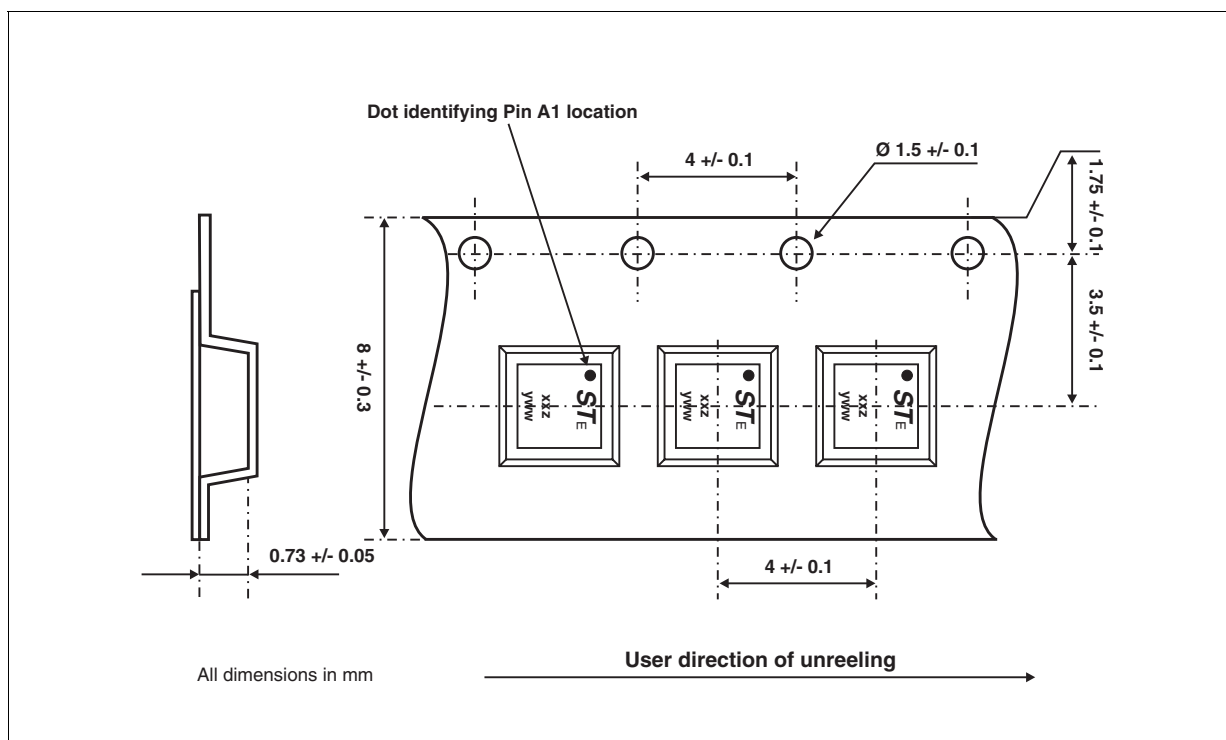


Figure 16: FLIP-CHIP Tape and Reel Specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Part Number	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-LCD01C2	FL	Flip-Chip	9.3 mg	5000	Tape & reel (7")

Table 4: Ordering Information

Note: Further packing information available in the application notes
 - AN1235: "Flip-Chip: Package description and recommendations for use"
 - AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
12-Aug-2005	1	First issue

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