ISD Cortex™-M0 ChipCorder

ISD9300 Series

Datasheet

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1 GENERAL DESCRIPTION

The ISD9300 is a system-on-chip product optimized for low power, audio record and playback with an embedded ARM® Cortex™-M0 32-bit microcontroller core.

The ISD9300 embeds a Cortex™-M0 core running up to 98 MHz with 68/100/145K-byte of non-volatile flash memory and 16K-byte of embedded SRAM. It also comes equipped with a variety of peripheral devices, such as Timers, Watchdog Timer (WDT), Real-time Clock (RTC), Peripheral Direct Memory Access (PDMA), a variety of serial interfaces (UART, SPI/SSP, I^2C, I^2S), PWM modulators, GPIO, Analog Comparator, Low Voltage Detector and Brown-out detector.

The ISD9300 comes equipped with a rich set of power saving modes including a Deep Power Down (DPD) mode drawing less than 1μA. A micro-power 16 KHz oscillator can periodically wake up the device from deep power down to check for other events. A Standby Power Down (SPD) mode can maintain a real time clock function at less than 10 μA.

For audio functionality the ISD9300 includes a Sigma-Delta ADC with 90dB SNR performance coupled with a Programmable Gain Amplifier (PGA) capable of a maximum gain of 61dB to enable direct connection of a microphone. Audio output is provided by a Differential Class D amplifier (DPWM) that can deliver 1W[1] of power to an 8Ω speaker.

The ISD9300 provides 16 analog enabled general purpose IO pins (GPIO). These pins can be configured to connect to an analog comparator, or can be configured as analog current sources. They can also be used as a relaxation oscillator to perform capacitive touch sensing. 8 of these 16 pins can be routed to the SDADC for analog to digital conversion.

[1] We suggest implementing thermal protection by utilizing the Temperature Alarm; for details please refer to Temperature Alarm in Design Guide.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 98.304MHz.
  - One 24-bit System tick timer for operating system support.
  - Supports a variety of low power sleep and power down modes.
  - Single-cycle 32-bit hardware multiplier.
  - NVIC (Nested Vector Interrupt Controller) for 32 interrupt inputs, each with 4-levels of priority.
  - Serial Wire Debug (SWD) support with 2 watchpoints/4 breakpoints.
- Power Management
  - Wide operating voltage range from 2.4V to 5.5V.
  - Power management Unit (PMU) providing four levels of power control.
  - Deep Power Down (DPD) mode with sub micro-amp leakage (<1μA).
  - Wakeup from Deep Power Down via dedicated WAKEUP pin or timed operation from internal low power 16KHz oscillator.
  - Standby mode with limited RAM retention and RTC operation (<10μA).
  - Wakeup from Standby can be from any GPIO interrupt, RTC or BOD.
  - Sleep mode with minimal dynamic power consumption.
  - 3V LDO for operation of external 3V devices such as serial flash.
- Flash EPROM Memory
  - 68/100/145K bytes Flash EPROM for program code and data storage.
  - Pre-fetch and mini-cache for near zero-wait state memory access.
  - 4KB of flash can be configured as boot sector for ISP loader.
  - Support In-system program (ISP) and In-circuit program (ICP) application code update
  - 1K byte page erase for flash
  - Configurable boundary to delineate code and data flash.
  - Support 2 wire In-circuit Programming (ICP) update from SWD ICE interface
  - Pre-fetch and cache for near zero-wait state memory operation.
- SRAM Memory
  - 16K bytes embedded SRAM.
- Clock Control
  - One high speed and two low speed oscillators providing flexible selection for different applications. No external components necessary.
  - Built-in trimmable oscillator with range of 16-50MHz. Factory trimmed within 1% to settings of 98.304MHz. User trimmable with in-built frequency measurement block (OSCFM) using reference clock of 32kHz crystal or external reference source.
  - Ultra-low power (<1uA) 16kHz oscillator for watchdog and wakeup from power-down or sleep operation.
  - External 32kHz crystal input for RTC function and low power system operation.
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable.
  - I/O pin can be configured as interrupt source with edge/level setting.
  - Switchable pull-up.
- Audio Analog to Digital converter
  - Sigma Delta ADC with configurable decimation filter and 16 bit output.
  - 90dB Signal-to-Noise (SNR) performance.

- Programmable gain amplifier with 32 steps from -12 to 35.25dB in 0.75dB steps.
- Boost gain stage of 26dB, giving maximum total gain of 61dB.
- Input selectable from dedicated MIC pins or analog enabled GPIO.
- Programmable biquad filter to support multiple sample rates from 8-32kHz.
- DMA support for minimal CPU intervention.

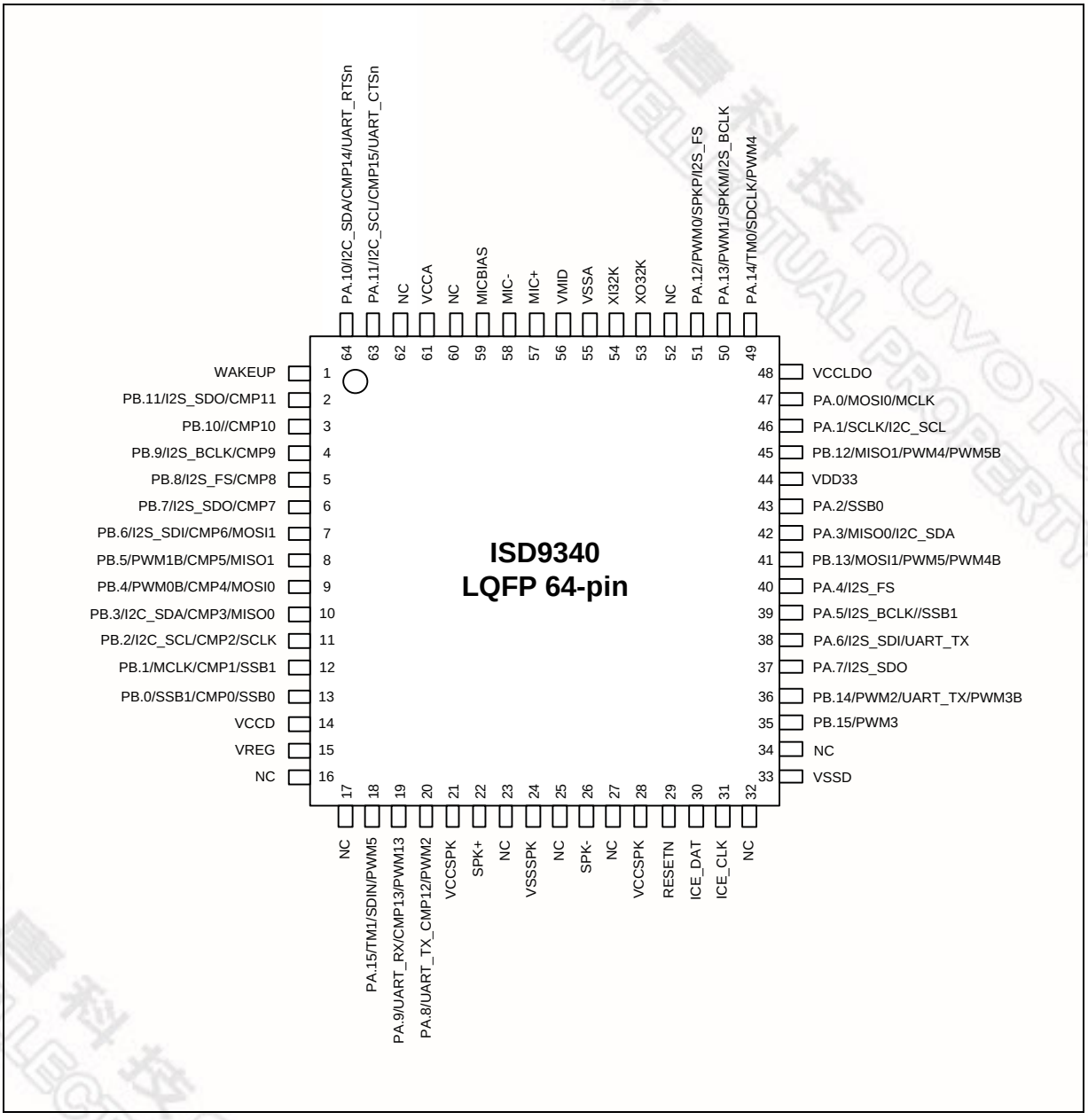
- Differential Audio PWM Output (DPWM)
  - Direct connection of speaker
  - 1W drive capability into 8Ω load.
  - High efficiency 88%
  - Configurable up-sampling to support sample rates from 8-32kHz.
  - DMA support for minimal CPU intervention.
- Timers
  - Two timers with 8-bit pre-scaler and 24-bit resolution.
  - Counter auto reload.
- Watch Dog Timer
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from micro seconds to seconds (depending on clock source)
  - WDT can wake up sleep.
  - Interrupt or reset selectable on watchdog time-out.
- RTC
  - Real Time Clock counter (second, minute, hour) and calendar counter (day, month, year)
  - Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Time tick and alarm interrupts.
  - Device wake up function.
  - Supports software compensation of crystal frequency by compensation register (FCR)
- PWM/Capture
  - Six 16-bit PWM generators provide six single ended PWM outputs or three complementary paired PWM outputs.
  - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scaler and Dead-Zone generator for complementary paired PWM.
  - PWM interrupt synchronous to PWM period.
  - 16-bit digital Capture timers (shared with PWM timers) provide rising/falling capture inputs.
  - Support Capture interrupt
- UART
  - UART ports with flow control (TX, RX, CTS and RTS)
  - 8-byte FIFO.
  - Support IrDA (SIR) and LIN function
  - Programmable baud-rate generator up to 1/16 of system clock.
- SPI
  - SPI clock up to 24MHz.
  - SPI data rate in Quad mode up to 98Mbps.
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 4 bytes.
  - MSB or LSB first data transfer
  - 2 slave/device select lines when used in master mode.
  - Hardware CRC calculation module available for CRC calculation of data stream.
  - DMA support for burst transfers.
  - Dual/Quad SPI support.

- I2C
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
  - Programmable clock allowing versatile rate control.
  - I2C-bus controller supports multiple address recognition.
- I^2S
  - Interface with external audio CODEC
  - Operate as either master or slave
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports DMA requests, for transmit and receive
- Brown-out detector
  - With 16 levels: 2.3V, 2,4V, 2.6V, 2.7V, 2.8V, 3.0V, 3.2V, 3.3V, 3.4V, 3.6V, 3.8V, 3.9V, 4.0V, 4.1V, 4.4V, 4.8V.
  - Supports time-multiplex operation to minimize power consumption
  - Supports Brownout Interrupt and Reset option
- Built in Low Dropout Voltage Regulator (LDO)
  - Capable of delivering 30mA load current.
  - Configurable for output voltage of 1.8V, 2.4V, 3.0V and 3.3V
  - Eight GPIO (GPIOA<7:0>) operate from LDO voltage domain allowing direct interface to, for example, 3V SPI Flash.
  - Can be bypassed and voltage domain supplied directly from system power.
- Additional Features
  - Over temperature alarm. Can generate interrupt if device exceeds safe operating temperature.
  - Temperature proportional voltage source which can be routed to ADC for temperature measurements.
  - Digital Microphone interface.
- Operating Temperature: -40C~85C
- Package:
  - All Green package (RoHS)
    - LQFP 64-pin

3 PART INFORMATION AND PIN CONFIGURATION

3.1 Pin Configuration

3.1.1 ISD9300 LQFP 64 pin



3.1.2 Pin Description

The ISD9300 is a low pin count device where many pins are configurable to alternative functions. All General Purpose input/output (GPIO) pins can be configured to alternate functions as described in the table below.

Pin No. LQFP 64	Pin Name	Pin Type	Alt CFG	Description
1	WAKEUP	**I**		Pull low to wake part from deep power down
2	PB.11	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 11
	I2S_SDO	**O**	1	I2S Serial Data Output
	CMP11	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
3	PB.10	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 10
	CMP10	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
4	PB.9	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 9
	I2S_BCLK	**O**	1	I2S Bit Clock (master mode only)
	CMP9	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
5	PB.8	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 8
	I2S_FS	**O**	1	I2S Frame Sync (master mode only)
	CMP8	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
6	PB.7	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 7
	I2S_SDO	**I/O**	1	I2S Serial Data Output
	CMP7	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
7	PB.6	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 6
	I2S_SDI	**I/O**	1	I2S Serial Data Input
	CMP6	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MOSI1	**O**	3	SPI interface Channel 1 Master Out, Slave In
8	PB.5	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 5.
	PWM1B	**O**	1	PWM channel 1 complementary Output
	CMP5	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MISO1	**O**	3	SPI Channel 1 Master In, Slave Out
9	PB.4	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 4.
	PWM0B	**O**	1	PWM Channel 0 complementary Output
	CMP4	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MOSI0	**I/O**	3	SPI Channel 0 Master Out, Slave In

Pin No. LQFP 64	Pin Name	Pin Type	Alt CFG	Description
10	PB.3	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 3
	I2C_SDA	**I/O**	1	I2C Serial Data
	CMP3	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_MISO0	**I/O**	3	SPI Channel 0 Master In, Slave Out
11	PB.2	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 2
	I2C_SCL	**I/O**	1	I2C Serial Clock
	CMP2	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_SCLK	**O**	3	SPI Serial Clock
12	PB.1	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 1. External interrupt 1 (EINT/IRQ3) trigger pin.
	MCLK	**O**	1	Master clock output for synchronizing external device
	CMP1	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_SSB1	**O**	3	Slave Select Bar 1 for SPI interface
13	PB.0	**A/I/O**	0	General purpose input/output pin, analog capable; Port B, bit 0. External interrupt 0 (EINT/IRQ2) trigger pin.
	SPI_SSB1	**O**	1	Slave Select Bar 1 for SPI interface
	CMP0	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	SPI_SSB0	**I/O**	3	Slave Select Bar 0 for SPI interface
14	VCCD	**P**		Main Digital Supply for Chip. Supplies all IO except analog, Speaker Driver, PA<0:7> and PB<12:13>.
15	VREG	**P**		Logic regulator output decoupling pin. A 1µF capacitor returning to VSSD must be placed on this pin.
16	NC			Should remain unconnected.
17	NC			Should remain unconnected.
18	PA.15	**I/O**	0	General purpose input/output pin; Port A, bit 15
	TM1	**I**	1	External input to Timer 1
	SDIN	**I**	2	Sigma Delta bit stream input for digital MIC mode
	PWM5	**O**	3	PWM5 Output
19	PA.9	**A/I/O**	0	General purpose input/output pin, analog capable; Port A, bit 9.
	UART_RX	**I**	1	Receive channel of UART
	CMP13	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	PWM3	**O**	3	PWM3 Output
20	PA.8	**A/I/O**	0	General purpose input/output pin, analog capable; Port A, bit 9.

Pin No. LQFP 64	Pin Name	Pin Type	Alt CFG	Description
	UART_TX	**O**	1	Transmit channel of UART
	CMP12	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	PWM2	**O**	3	PWM2 Output
21	VCCSPK	**P**		Power Supply for PWM Speaker Driver
22	SPK+	**O**		Positive Speaker Driver Output
23	NC			Should remain unconnected.
24	VSSSPK	**P**		Ground for PWM Speaker Driver
25	NC			Should remain unconnected.
26	SPK-	**O**		Negative Speaker Driver Output
27	NC			Should remain unconnected.
28	VCCSPK	**P**		Power Supply for PWM Speaker Driver
29	RESETN	**I**		External reset input. Pull this pin low to reset device to initial state. Has internal weak pull-up.
30	ICE_DAT	**I/O**		Serial Wire Debug port data pin. Has internal weak pull-up.
31	ICE_CLK	**I**		Serial Wire Debug port clock pin. Has internal weak pull-up.
32	NC			Should remain unconnected.
33	VSSD	**P**		Digital Ground.
34	NC			Should remain unconnected.
35	PB.15	**I/O**	0	General purpose input/output pin; Port B, bit 15.
	PWM3	**O**	1	PWM3 Output.
	PWM2B	**O**	3	PWM channel 2 complementary Output
36	PB.14	**I/O**	0	General purpose input/output pin; Port B, bit 14.
	PWM2	**O**	1	PWM2 Output.
	UART_TX	**O**	2	UART Transmit
	PWM3B	**O**	3	PWM channel 3 complementary Output
37	PA.7	**I/O**	0	General purpose input/output pin; Port A, bit 7
	I2S_SDO	**O**	1	I2S Serial Data Output
38	PA.6	**I/O**	0	General purpose input/output pin; Port A, bit 6
	I2S_SDI	**I**	1	I2S Serial Data Input
	UART_TX	**O**	2	UART Transmit
39	PA.5	**I/O**	0	General purpose input/output pin; Port A, bit 5
	I2S_BCLK	**I/O**	1	I2S Bit Clock

Pin No. LQFP 64	Pin Name	Pin Type	Alt CFG	Description
	SPI_SSB1	**O**	3	SPI Slave Select 1
40	PA.4	**I/O**	0	General purpose input/output pin; Port A, bit 4
	I2S_FS	**I/O**	1	I2S Frame Sync
41	PB.13	**I/O**	0	General purpose input/output pin; Port B, bit 13.
	SPI_MOSI1	**O**	1	SPI Channel 1 Master Out, Slave In
	PWM5	**O**	2	PWM5 Output
	PWM4B	**O**	3	PWM Channel 4 Complementary Output
42	PA.3	**I/O**	0	General purpose input/output pin; Port A, bit 3
	SPI_MISO0	**I**	1	SPI Channel 0 Master In, Slave Out
	I2C_SDA	**I/O**	2	I2C Serial Data
43	PA.2	**I/O**	0	General purpose input/output pin; Port A, bit 2
	SPI_SSB0	**I/O**	1	SPI Slave Select 0
44	VDD33	**P**		LDO Regulator Output. If used, a 1µF capacitor must be placed to ground. If not used then tie to VCCD.
45	PB.12	**I/O**	0	General purpose input/output pin; Port B, bit 13.
	SPI_MISO1	**O**	1	Master In, Slave Out channel 1 for SPI interface
	PWM4	**O**	2	PWM4 Output
	PWM5B	**O**	3	PWM channel 5 Complementary Output
46	PA.1	**I/O**	0	General purpose input/output pin; Port A, bit 1
	SPI_SCLK	**I/O**	1	SPI Serial Clock
	I2C_SCL	**I/O**	2	I2C Serial Clock
47	PA.0	**I/O**	0	General purpose input/output pin; Port A, bit 2
	SPI_MOSI0	**O**	1	SPI Channel 0 Master Out, Slave In
	MCLK	**O**	2	Master clock output.
48	VCCLDO	**P**		Power Supply for LDO, should be connected to VCCD
49	PA.14	**I/O**	0	General purpose input/output pin; Port A, bit 14
	TM0	**I**	1	External input to Timer 0
	SDCLK	**O**	2	Inverse Clock output for digital microphone mode.
	PWM4	**O**	3	PWM4 Output
50	PA.13	**I/O**	0	General purpose input/output pin; Port A, bit 13
	PWM1	**O**	1	PWM1 Output.
	SPKM	**O**	2	Equivalent to SPK-.

Pin No. LQFP 64	Pin Name	Pin Type	Alt CFG	Description
	I2S_BCLK	**I/O**	3	I2S Bit Clock
51	PA.12	**I/O**	0	General purpose input/output pin; Port A, bit 12
	PWM0	**O**	1	PWM0 Output.
	SPKP	**O**	2	Equivalent to SPK+
	I2S_FS	**I/O**	3	I2S Frame Sync
52	NC			Should remain unconnected.
53	XO32K	**O**		32.768kHz Crystal Oscillator Output
54	XI32K	**I**		32.768kHz Crystal Oscillator Input. Max Voltage 1.8V
55	VSSA	**AP**		Ground for analog circuitry.
56	VMID	**O**		Mid rail reference. Connect 4.7µF to VSSA.
57	MIC+	**AI**		Positive microphone input.
58	MIC-	**AI**		Negative microphone input.
59	MICBIAS	**AO**		Microphone bias output.
60	NC			Should remain unconnected.
61	VCCA	**AP**		Analog power supply.
62	NC			Should remain unconnected.
63	PA.11	**A/I/O**	0	General purpose input/output pin, analog capable; Port A, bit 11
	I2C_SCL	**I/O**	1	I2C Serial Clock
	CMP15	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	UART_CTSn	**I**	3	UART Clear to Send Input.
64	PA.10	**A/I/O**	0	General purpose input/output pin, analog capable; Port A, bit 10
	I2C_SDA	**I/O**	1	I2C Serial Data
	CMP14	**AIO**	2	Configure as relaxation oscillator for capacitive touch sensing
	UART_RTSn	**O**	3	UART Request to Send Output.

Note:

- Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

4 BLOCK DIAGRAM

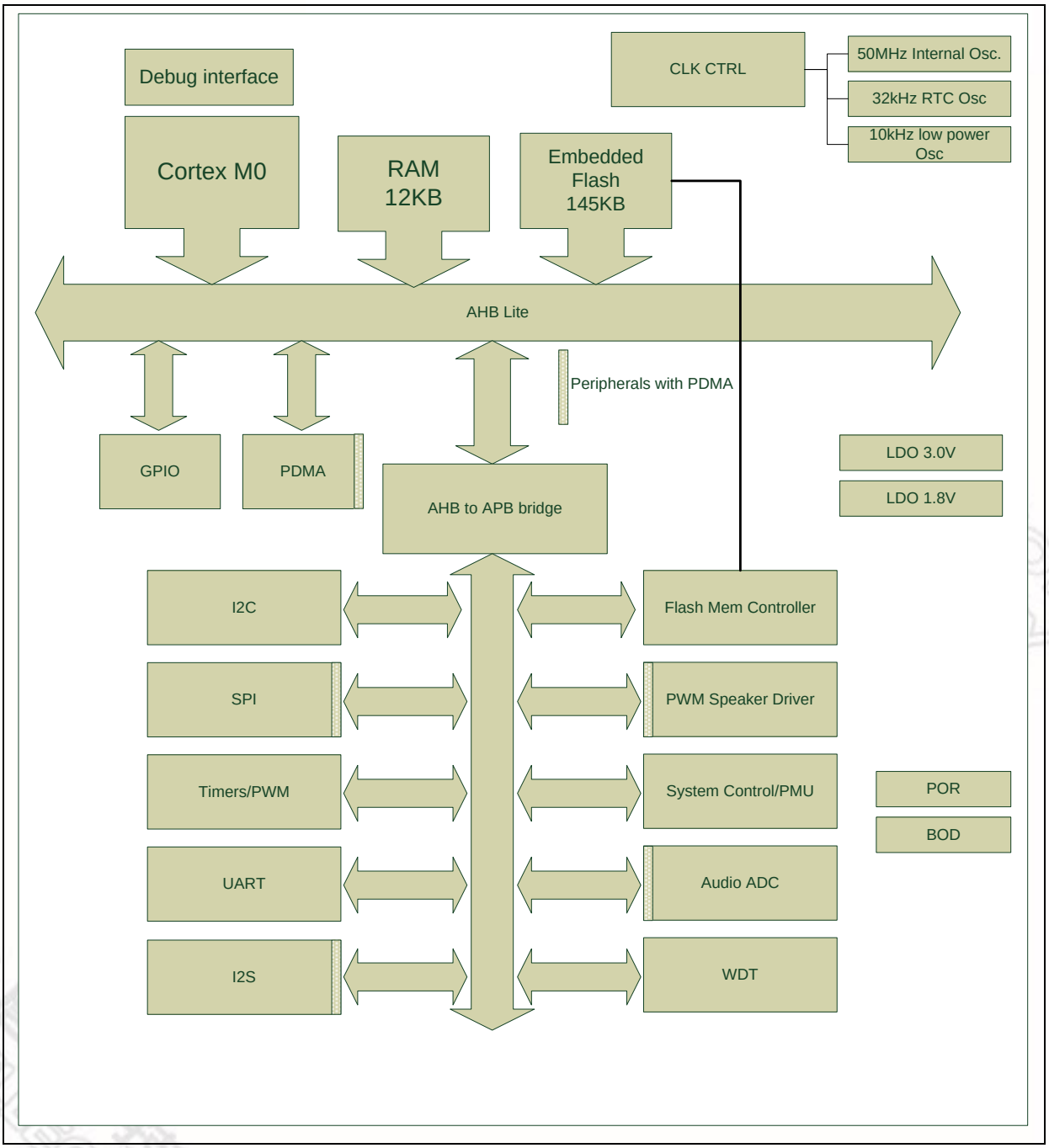
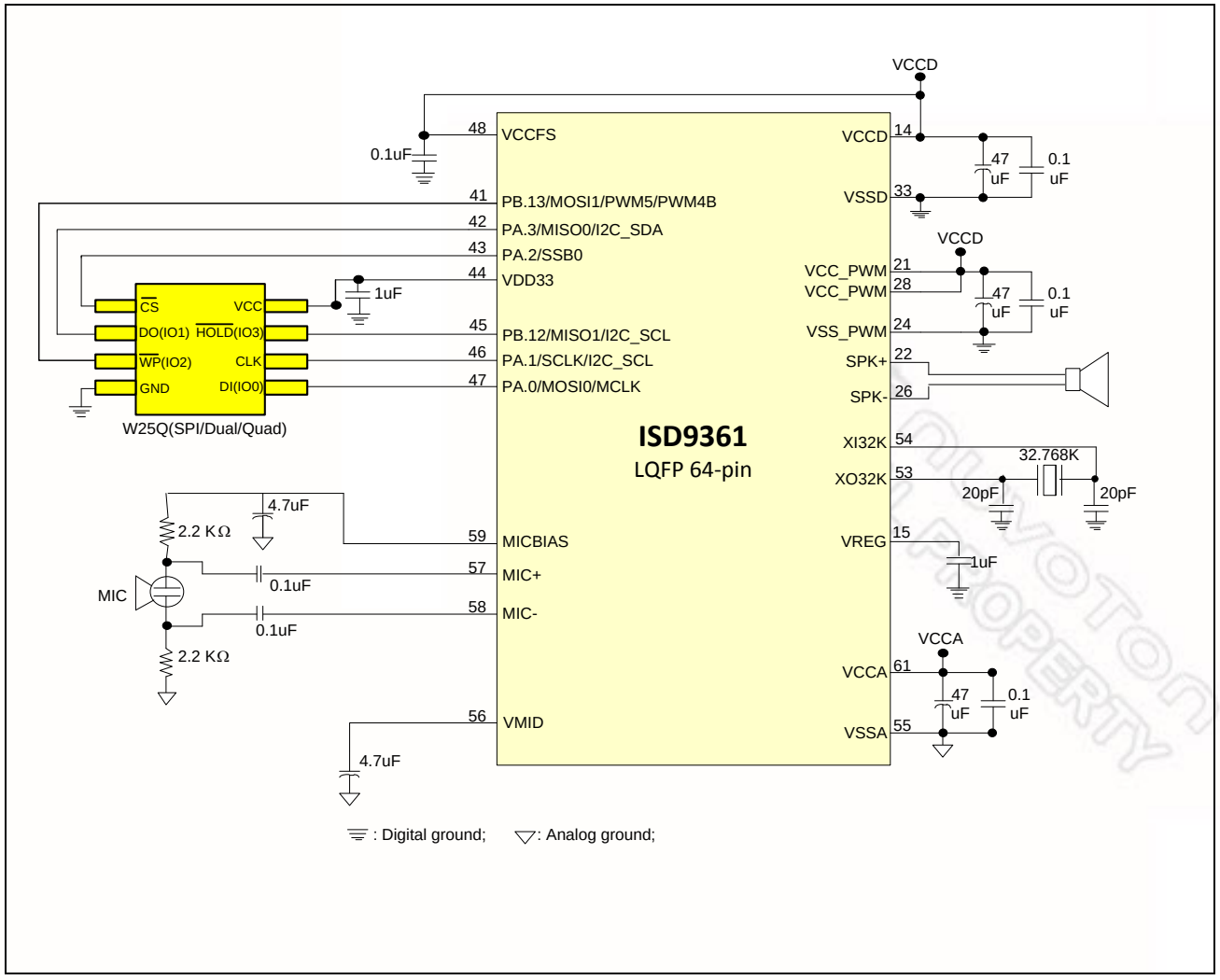


Figure 4-1 ISD9300 Block Diagram

5 APPLICATION DIAGRAM



6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+6.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	0	40	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.2 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, F_{OSC} = 49.152 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.4		5.5	V	V_{DD} =2.4V ~ 5.5V up to 100 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
DPWM Speaker Voltage	V_{DDspk}	2.4		5.5	V	
Current Consumption @ Normal Mode @ 49.152 MHz	I_{DD}		25		mA	V_{DD}= 5.5V
	I_{DD}		21		mA	V_{DD} = 3V
Current Consumption @ Sleep Mode	I_{IDLE1}		10		mA	V_{DD}= 5.5V, Enable all IP (analog and digital)
	I_{IDLE1}		9		mA	V_{DD}= 3.3V, Enable all IP (analog and digital)

Current Consumption @ Deep Sleep Mode	I_{IDLE1}		10		mA	V_{DD}=5.5V. *
	I_{IDLE1}		9		mA	V_{DD}= 3.3V. *
Current Consumption @ Standby Power Down Mode(SPD)	I_{IDLE1}		5		uA	V_{DD}=3.3V, 32K CRTL running with RTC
	I_{IDLE1}		1		uA	V_{DD}= 3.3V, OSC16K
Current Consumption @ Deep Power Down Mode(DPD)	I_{IDLE1}		400		nA	V_{DD}=3.3V, Wakeup by OSC16K timer
	I_{IDLE1}		500		nA	V_{DD}= 3.3V, wakeup by Wakeup pin

*: Data value for this item varies depending on different IP module enabled.

Input Current PA, PB (Quasi-bidirectional mode)	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at /RESET [1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PB (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.51	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	V	
Input High Voltage X32I[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /REST	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input), /REST	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage of PA~PB(Schmitt input)	V_{HY}		0.2V_{DD}		V	

Source Current PA, PB Quasi-bidirectional Mode)	I_{SR11}	-300	-340	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-65	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-55	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-3.54	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	12	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	9	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	7	12	mA	V_{DD} = 2.5V, V_S = 0.45V

Note:

1. /REST pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when Vin approximates to 2V.

6.3 AC Electrical Characteristics

6.3.1 External 32kHz XTAL Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.4	-	5.5	V

6.3.2 Internal 49.152MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.4	-	5.5	V
Center Frequency	-	-	49.152		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =3V	-1	-	1	%
	-40°C~+85°C; V_{DD}=2.4V~5.5V	-4	-	4	%

6.3.3 Internal 16 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.4	-	5.5	V
Center Frequency	-	-	16	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =3V	-10	-	10	%
	-40°C~+85°C; V_{DD}=2.4V~5.5V	-20	-	20	%

.

6.4 Analog Characteristics

6.4.1 Specification of ADC and Speaker Driver

Conditions: VCCD = 3.3V, VCCA = 3.3V, TA = 25°C, 1kHz signal, fs = 16kHz, 16-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted		90		dB
Total harmonic distortion [2]	THD+N	Input = -3dB FS input		0.04		%
PWM Speaker Output (8Ω bridge-tied-load)						
Full scale output [4]				VCCSPK / 3.3		V_{rms}
Total harmonic distortion [2]	THD+N	P_o= 200mW, VDDSPK=3.3V		*63		dB
		P_o= 320mW, VDDSPK = 3.3V		-64		dB
		P_o= 860mW, VDDSPK = 5V		-60		dB
		P_o= 1000mW, VDDSPK = 5V		-36		dB
Signal-to-noise ratio	SNR	VDDSPK = 3.3V		90		dB
		VDDSPK=5V		89		dB
Power supply rejection ratio (50Hz – 22kHz)	PSRR	VDDSPK = 3.3V		TBD		dB
		VDDSPK = 5V		TBD		dB

6.4.2 Specification of PGA and BOOST

Conditions: VCCD = 3.3V, VCCA = 3.3V, TA = 25°C, 1kHz signal, fs = 16kHz, 16-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Microphone Inputs (MICP, MICN) and Programmable Gain Amplifier (PGA)						
Full scale input signal [1]		PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Programmable gain			-12		35.25	dB
Programmable gain step size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				120		dB
Input resistance		Inverting Input PGA Gain = 35.25dB PGA Gain = 0dB PGA Gain = -12dB **Non-inverting Input**		 1.6 47 75 94		 kΩ kΩ kΩ kΩ
Input capacitance				10		pF
PGA equivalent input noise		0 to 20kHz, Gain set to 35.25dB		120		µV

6.4.3 Specification of ALC and MICBIAS

Conditions: VCCD = 3.3V, VCCA = 3.3V, TA = 25°C, 1kHz signal, fs = 16kHz, 16-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Automatic Level Control (ALC) & Limiter:						
Target record level			-22.5		-1.5	dBFS
Programmable gain			-12		35.25	dB
Gain hold time [3]	t_{HOLD}	Doubles every gain step, with 16 steps total	0 / 2.67 / 5.33 / … / 43691			ms
Gain ramp-up (decay) [3]	t_{DCY}	ALC Mode ALC = 0	4 / 8 / 16 / … / 4096			ms
		Limiter Mode ALC = 1	1 / 2 / 4 / … / 1024			ms
Gain ramp-down (attack) [3]	t_{ATK}	ALC Mode ALC = 0	1 / 2 / 4 / … / 1024			ms
		Limiter Mode ALC = 1	0.25 / 0.5 / 1 / … / 128			ms
Mute Attenuation				120		dB
Microphone Bias						
Bias voltage	$V_{MICBIAS}$		0.90, 0.65 ,0.75, 0.50, 2.4, 1.7,2.0			VDDA V
Bias current source	$I_{MICBIAS}$			3		mA
Output noise voltage	V_n	1kHz to 20kHz		14		nV/√Hz

Notes:

1. Full Scale is relative to the magnitude of VCCA and can be calculated as FS=VCCA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurement is at 3dB below full scale, unless otherwise noted.
3. Time values scale proportionally with HCLK. Complete descriptions and definitions for these values are contained in the detailed description of the ALC functionality.

6.4.4 Specification of LDO and Power Management

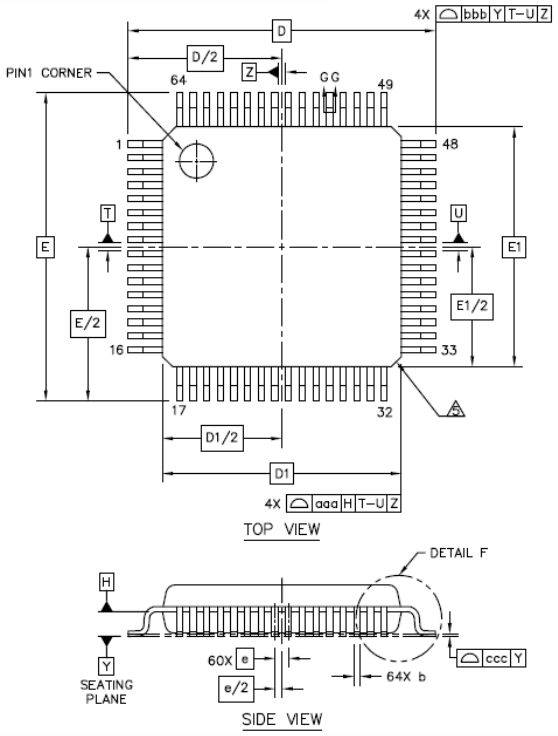
PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.4	5	5.5	V	V_{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	V_{DD}> 1.8

Note:

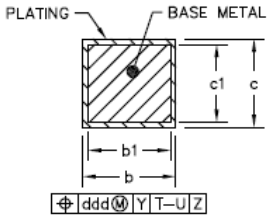
1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VCCD and the VSSD pin of the device.
2. To ensure regulator stability, a 1.0uF capacitor must be connected between LDO pin and the VSSD pin of the device. Also a 100nF bypass capacitor between LDO and VSSD will help suppress output noise.

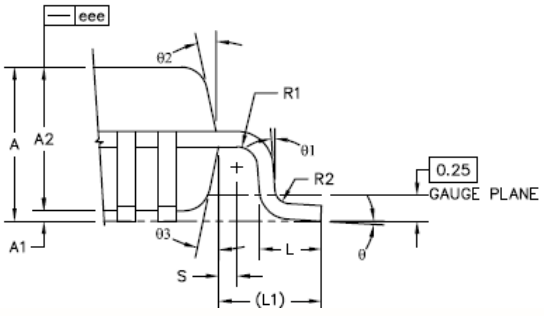
7 PACKAGE DIMENSIONS

7.1.1 64L LQFP (7x7x1.4mm footprint 2.0mm)

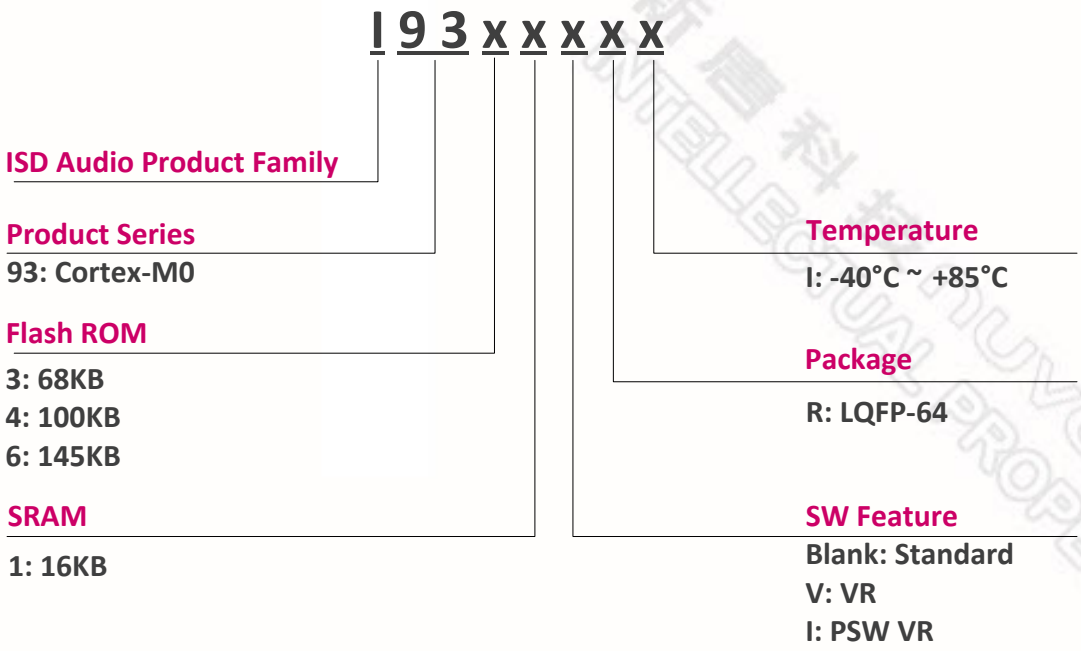


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





8 ORDERING INFORMATION



9 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V0.1	Dec 10, 2013	-	First preliminary Release.
V0.2	Jan 13, 2014	-	Description update
V1.0	Jan 23, 2014	-	Description update. Remove preliminary.
V1.1	Oct 23, 2014	-	Add ISD9331/9341 .into the ISD9300 series.

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